QuartzPro64 Dev Board Schematic

Main Functions Introduction

1) PMIC: 2xRK806-2+DiscretePower
2) RAM: 2xLPDDR4/4X_32bit
3) ROM: eMMC5.1(Default)+ SPI Falsh
4) Support: 1xVGA Connector
5) Support: 1 x USB3.0 HOST + 1 x TYPEC3.0+ 2 x USB20 HOST
6) Support: 1 x SATA3.0 Connector (7pin) + 4 pin Power Connector
7) Support: 1 x 4Lane PCIe3.0 Connector (Dual Mode)
8) Support: 4 x 2Lanes MIPI DPHY RX Camera(Need daughter Board)
9) Support: 2 x 4Lanes MIPI DCPHY RX Camera(Need daughter Board)
10) Support: 2 x HDMI2.0 TX
11) Support: 1 x HDMI2.0 RX
12) Support: 2 x 4Lanes MIPI DHY-TX
13) Support: a/b/g/n/ac/ax 2T2R WIFI 6+BT5.0(PCIE)
14) Support: 1x 10/100/1000 RJ45 Port(RGMII)
15) Support: 1x 10/100/1000 RJ45 Port(PCIE)
16) Support: 1xHeadphone+2xSPK+1xAnalog MIC
17) Support: 1xRecovery(VOL+)+1xReset+1xPower on+1xMenu+1xVOL-+1xESC
18) Support: 8 x SARADC
19) Support: Debug UART to USB connector and JTAG Connector

PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**00.Cover Page**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	1 of 44

Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

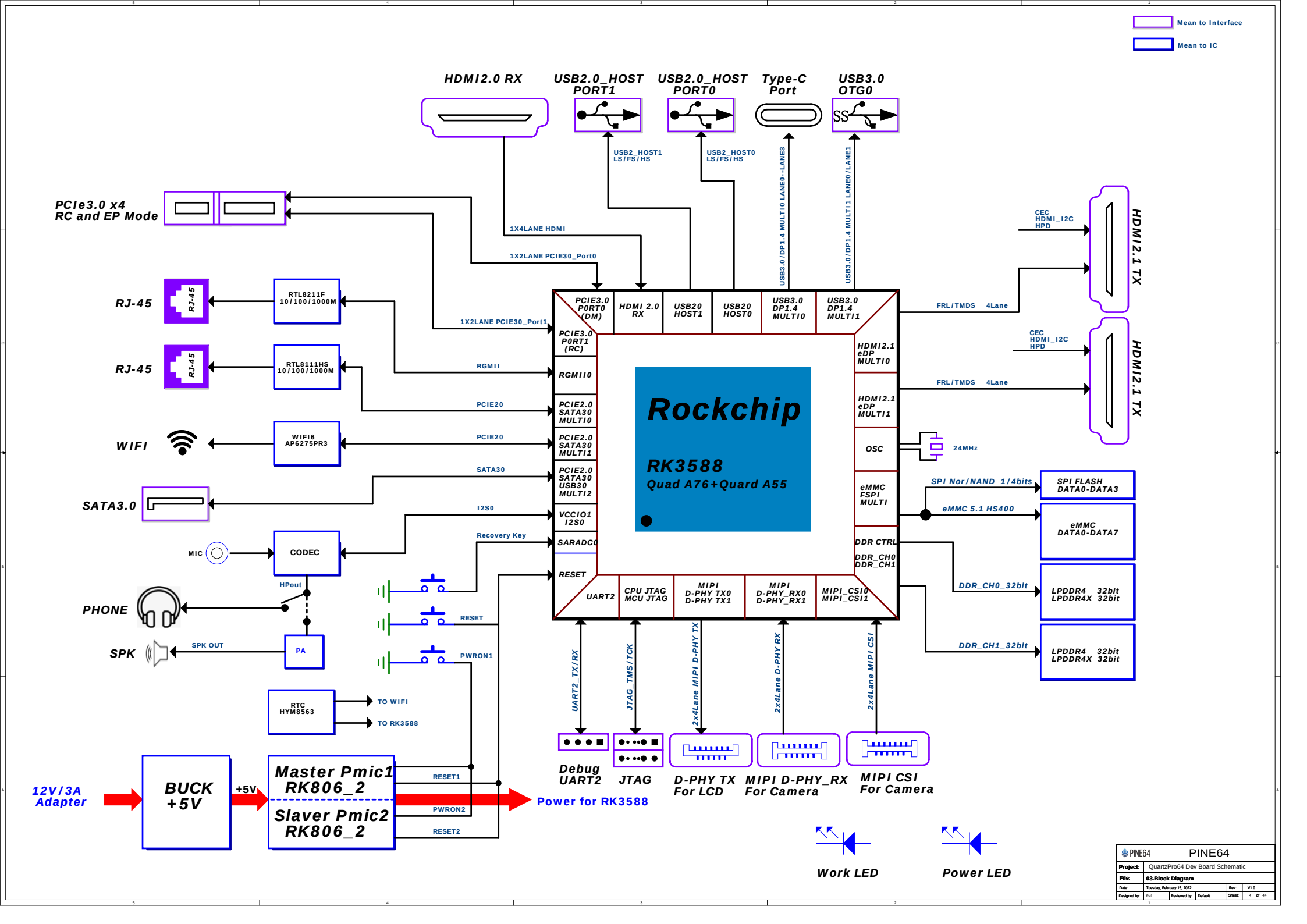
NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	01.Index and Notes				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	2 of 44

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2022-02-16	.ruan	1、Revision preliminary version	

PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**02.Revision History**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	3 of 44


Mean to Interface
Mean to IC
HDMI2.0 RX
USB2.0_HOST PORT1
USB2.0_HOST PORT0
Type-C Port
USB3.0 OTG0
USB2_HOST1 LS/FS/HS
USB2_HOST0 LS/FS/HS
USB3.0/DP1.4 MULTI0 LANE0--LANE3
USB3.0/DP1.4 MULTI1 LANE0/LANE1
PCIe3.0 x4 RC and EP Mode
1X4LANE HDMI
1X2LANE PCIE30_Port0
1X2LANE PCIE30_Port1
RGMII
PCIE20
PCIE20
SATA30
I2S0
Recovery Key
RESET
PWRON1
RJ-45
RJ-45
WIFI
SATA3.0
MIC
HPout
PHONE
SPK
SPK OUT
RTL8211F 10/100/1000M
RTL8111HS 10/100/1000M
WIFI6 AP6275PR3
CODEC
PA
RTC HYM8563
TO WIFI
TO RK3588
PCIE3.0 P0RT0 (DM)
HDMI 2.0 RX
USB20 HOST1
USB20 HOST0
USB3.0 DP1.4 MULTI0
USB3.0 DP1.4 MULTI1
PCIE3.0 P0RT1 (RC)
RGMII0
PCIE2.0 SATA30 MULTI0
PCIE2.0 SATA30 MULTI1
PCIE2.0 SATA30 USB30 MULTI2
VCCIO1 I2S0
SARADC0
RESET
HDMI2.1 eDP MULTI0
HDMI2.1 eDP MULTI1
OSC
eMMC FSPI MULTI
DDR CTRL
DDR_CH0
DDR_CH1
UART2
CPU JTAG MCU JTAG
MIPI D-PHY TX0 D-PHY TX1
MIPI D-PHY_RX0 D-PHY_RX1
MIPI_CSI0 MIPI_CSI1
Rockchip
RK3588
Quad A76+Quard A55
FRL/TMDS 4Lane
FRL/TMDS 4Lane
CEC HDMI_I2C HPD
CEC HDMI_I2C HPD
HDMI2.1 TX
HDMI2.1 TX
24MHz
SPI Nor/NAND 1/4bits
eMMC 5.1 HS400
DDR_CH0_32bit
DDR_CH1_32bit
SPI FLASH DATA0-DATA3
eMMC DATA0-DATA7
LPDDR4 32bit LPDDR4X 32bit
LPDDR4 32bit LPDDR4X 32bit
UART2_TX/RX
JTAG_TMS/TCK
2x4Lane MIPI D-PHY TX
2x4Lane D-PHY RX
2x4Lane MIPI CSI
Debug UART2
JTAG
D-PHY TX For LCD
MIPI D-PHY_RX For Camera
MIPI CSI For Camera
12V/3A Adapter
BUCK +5V
+5V
Master Pmic1 RK806_2
Slaver Pmic2 RK806_2
RESET1
PWRON2
RESET2
Power for RK3588
Work LED
Power LED
PINE64
Project: QuartzPro64 Dev Board Schematic
File: 03.Block Diagram
Date: Tuesday, February 15, 2022
Rev: V1.0
Designed by: Rzt
Reviewed by: Default
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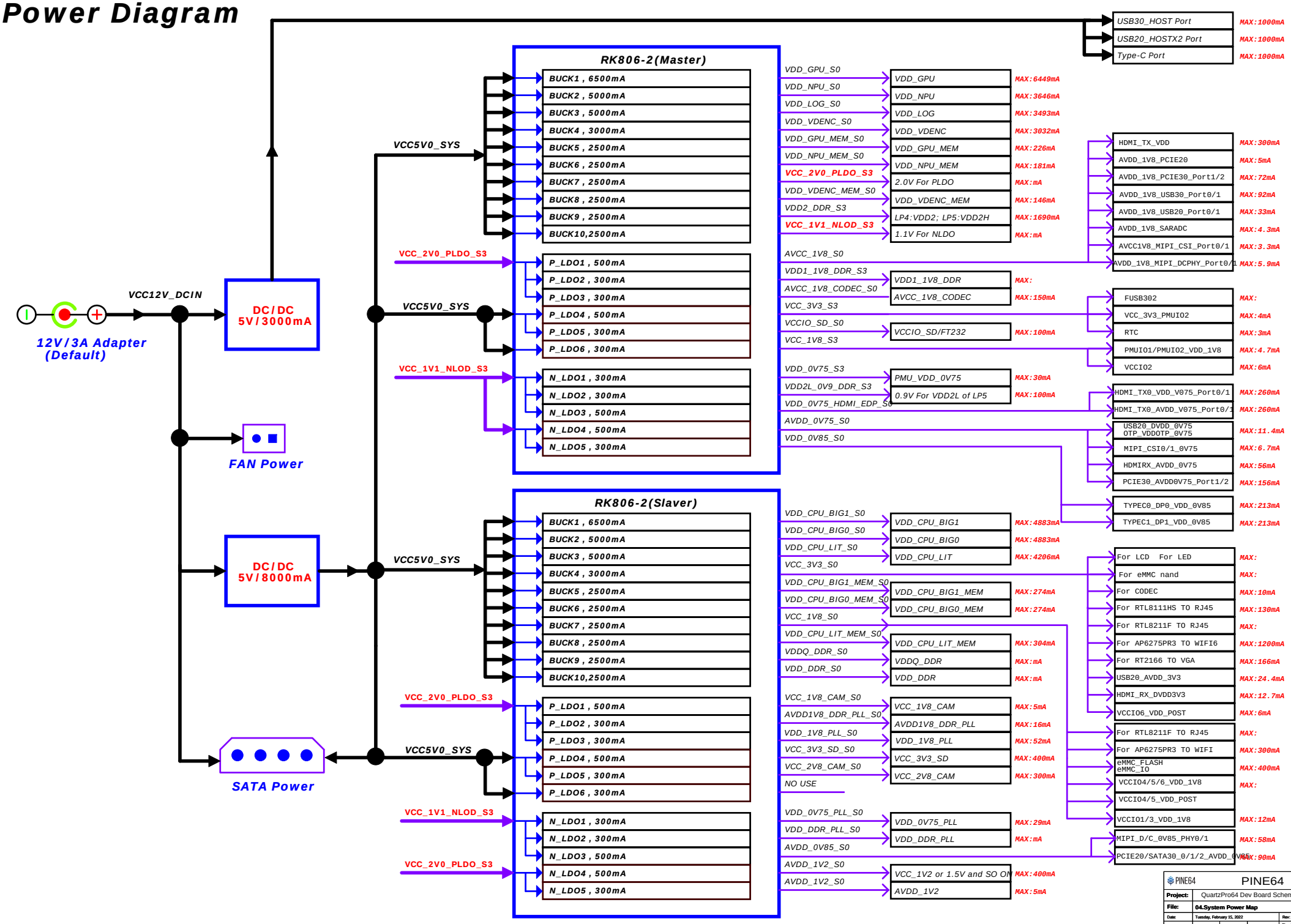
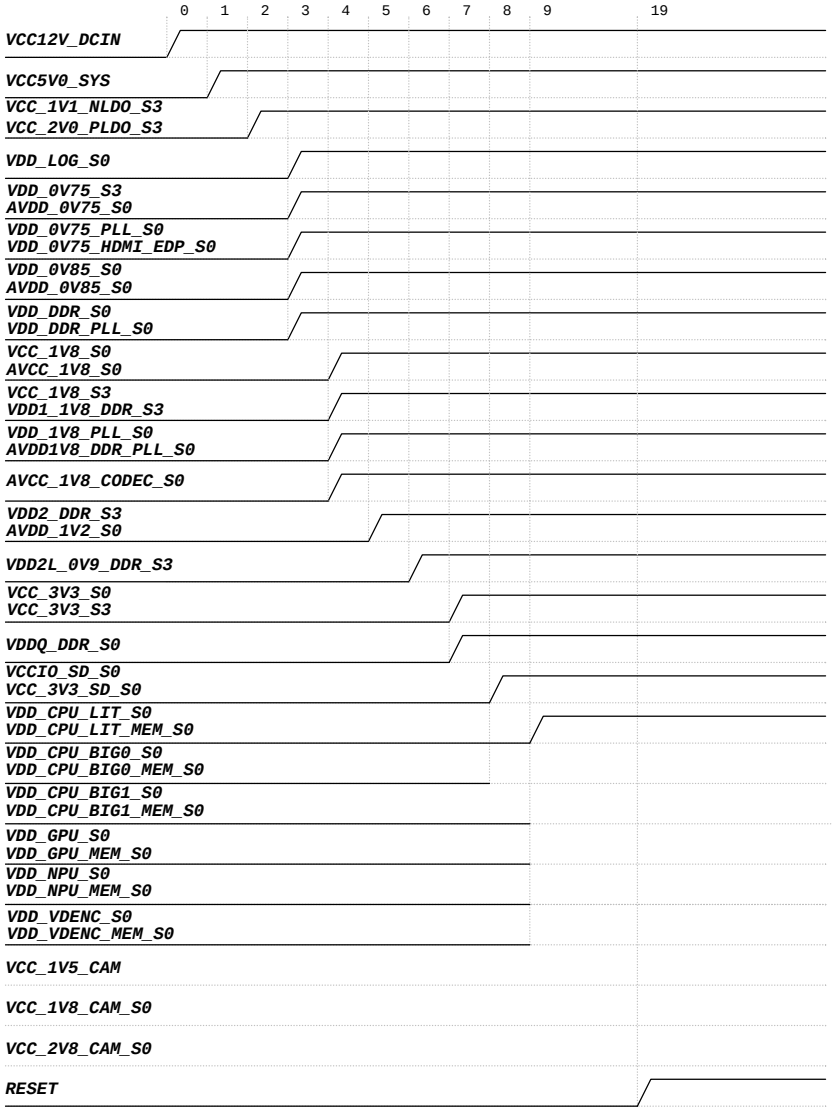
Power Diagram



Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC5V0_SYS	PMIC1_BUCK1	6.5A	VDD_GPU_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK2	5A	VDD_NPU_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK3	5A	VDD_LOG_S0		0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK4	3A	VDD_VDENC_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK5	2.5A	VDD_GPU_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK6	2.5A	VDD_NPU_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK7	2.5A	VCC_2V0_PLDO_S3		2.0V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK8	2.5A	VDD_VDENC_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK9	2.5A	VDD2_DDR_S3		1.1V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK10	2.5A	VCC_1V1_NLDO_S3		1.1V	ON	ON	TBD	TBD
VCC_2V0_PLDO	PMIC1_PLDO1	0.3A	AVCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
	PMIC1_PLDO2	0.3A	VDD1_1V8_DDR_S3		1.8V	ON	ON	TBD	TBD
	PMIC1_PLDO3	0.5A	AVCC_1V8_CODEC_S0		1.8V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_PLDO4	0.5A	VCC_3V3_S3		3.3V	ON	ON	TBD	TBD
	PMIC1_PLDO5	0.3A	VCCIO_SD_S0		3.3V	ON	OFF	TBD	TBD
VCC5V0_VCCA	PMIC1_PLDO6	0.3A	VCC_1V8_S3		1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO1	0.3A	VDD_0V75_S3		0.75V	ON	ON	TBD	TBD
	PMIC1_NLDO2	0.3A	VDD2L_0V9_DDR_S3		0.9V	ON	ON	TBD	TBD
	PMIC1_NLDO3	0.5A	VDD_0V75_HDMI_EDP_S0		0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO4	0.5A	AVDD_0V75_S0		0.75V	ON	OFF	TBD	TBD
	PMIC1_NLDO5	0.3A	VDD_0V85_S0		0.85V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK1	6.5A	VDD_CPU_BIG1_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK2	5A	VDD_CPU_BIG0_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK3	5A	VDD_CPU_LIT_S0		0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK4	3A	VCC_3V3_S0		3.3V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK5	2.5A	VDD_CPU_BIG1_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK6	2.5A	VDD_CPU_BIG0_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK7	2.5A	VCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK8	2.5A	VDD_CPU_LIT_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK9	2.5A	VDDQ_DDR_S0		0.6V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK10	2.5A	VDD_DDR_S0		0.85V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_PLDO1	0.3A	VCC_1V8_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_PLDO2	0.3A	AVDD1V8_DDR_PLL_S0		1.8V	ON	OFF	TBD	TBD
	PMIC2_PLDO3	0.5A	VDD_1V8_PLL_S0		1.8V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_PLDO4	0.5A	VCC_3V3_SD_S0		3.3V	ON	OFF	TBD	TBD
	PMIC2_PLDO5	0.3A	VCC_2V8_CAM_S0		0V	OFF	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC2_NLDO1	0.3A	VDD_0V75_PLL_S0		0.75V	ON	OFF	TBD	TBD
	PMIC2_NLDO2	0.3A	VDD_DDR_PLL_S0		0.85V	ON	OFF	TBD	TBD
	PMIC2_NLDO3	0.5A	AVDD_0V85_S0		0.85V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_NLDO4	0.5A	VCC_1V2_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_NLDO5	0.3A	AVDD_1V2_S0		1.2V	ON	OFF	TBD	TBD

IO Power Domain Map

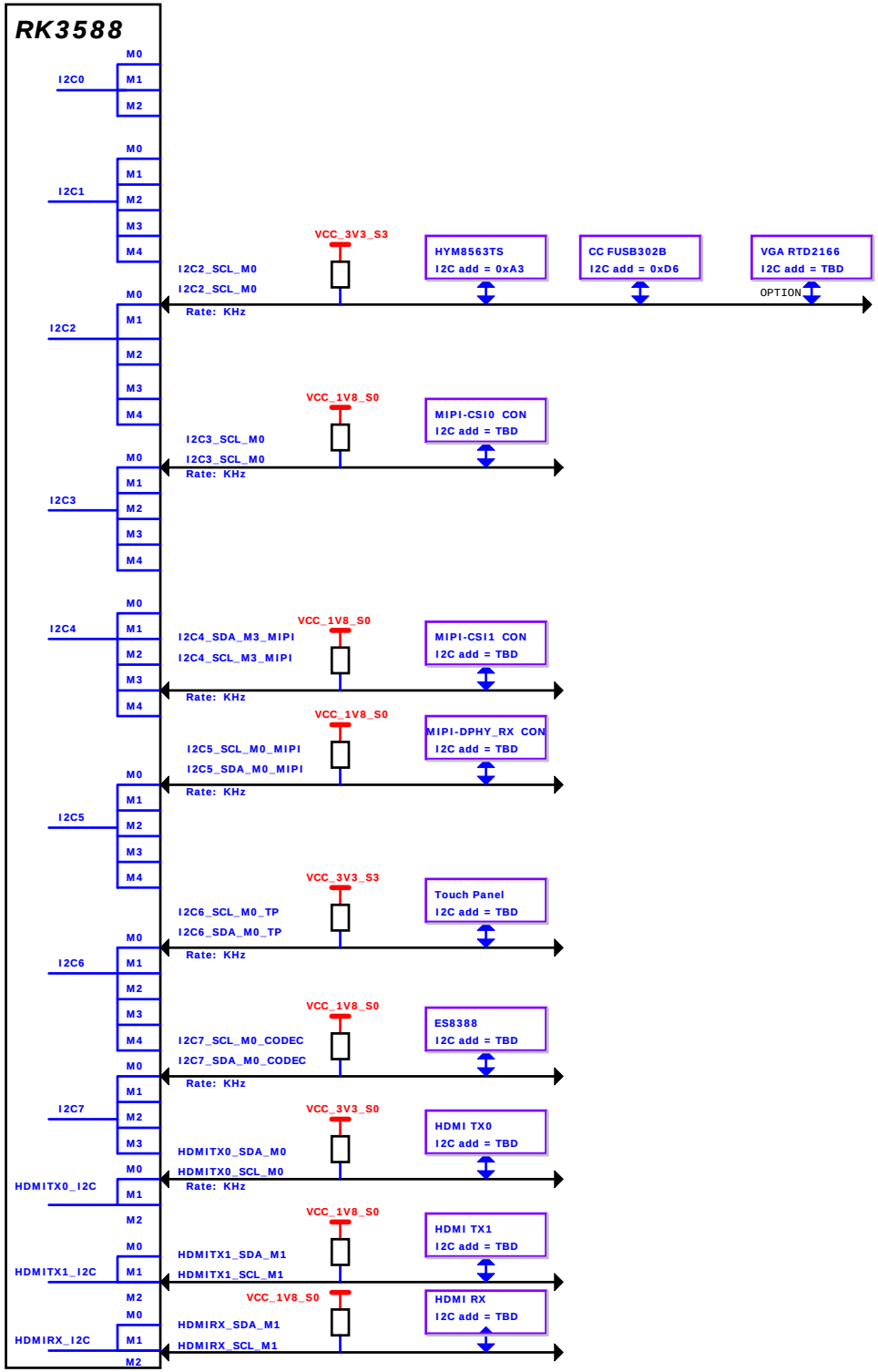
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_3V3_S3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VDDIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VDDIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_1V8/3V3_S0	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VDDIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VDDIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VDDIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VDDIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

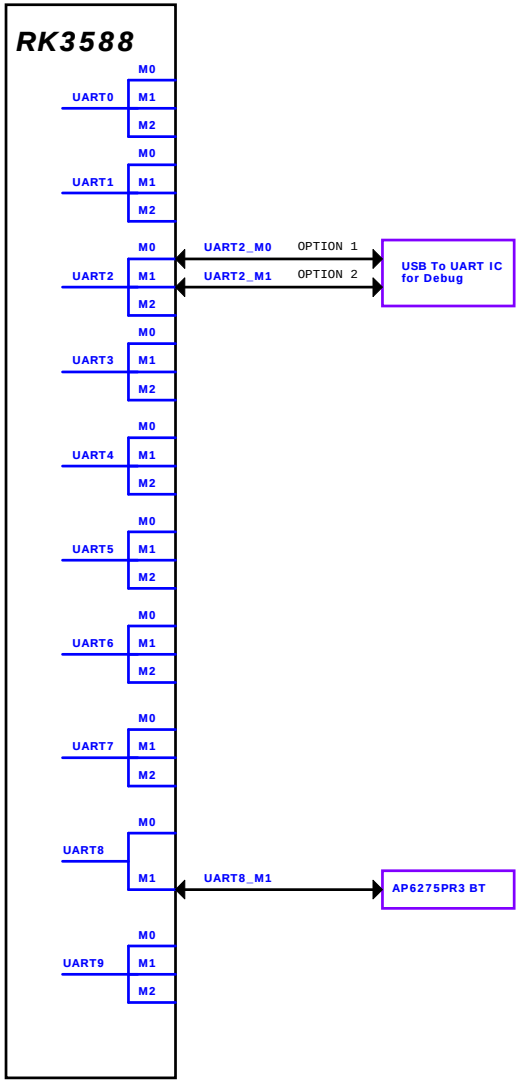
PINE64 PINE64

Project:	QuartzPro64 Dev Board Schematic				
File:	05.Power Sequence/IO Power				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	6 of 44

I2C MAP



UART MAP



PINE64	PINE64
Project:	QuartzPro64 Dev Board Schematic
File:	06.Lower-Speed Bus Map
Date:	Tuesday, February 15, 2022
Rev:	V0.1
Designed by:	Rtf
Reviewed by:	
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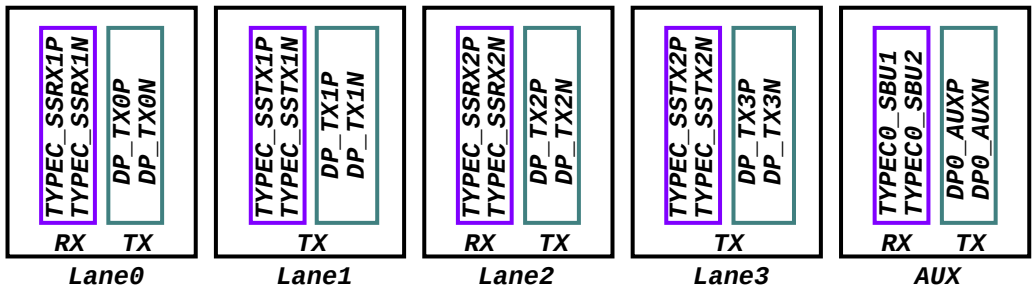
USB Controller Configure Table

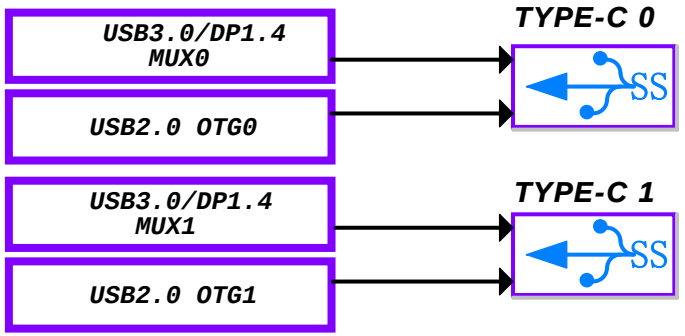
Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1N/DP1_TX1N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST	USB30 HOST				
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN				
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN				
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					
						TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM				

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

USB3.0/DP1.4 Lane Diagram

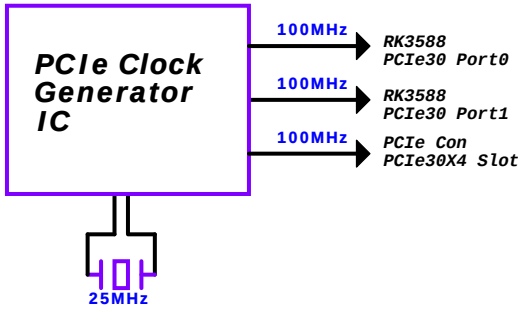


TYPE-C Connector Diagram

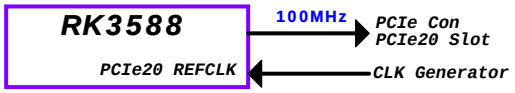


PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	07.USB Controller Configure Tab		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by: Rzf	Reviewed by:	Sheet:	8 of 44

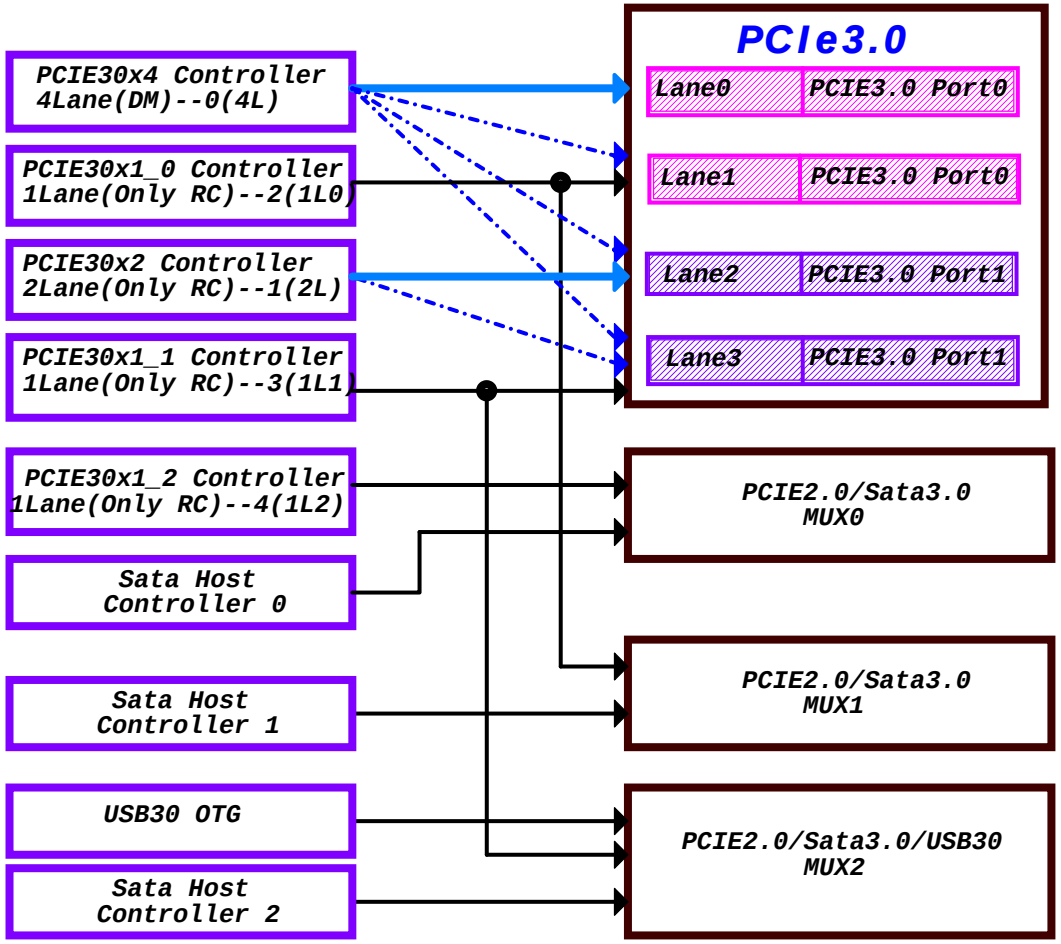
PCIe3.0 REFCLK



PCIe2.0 REFCLK



PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	
PCIE30X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

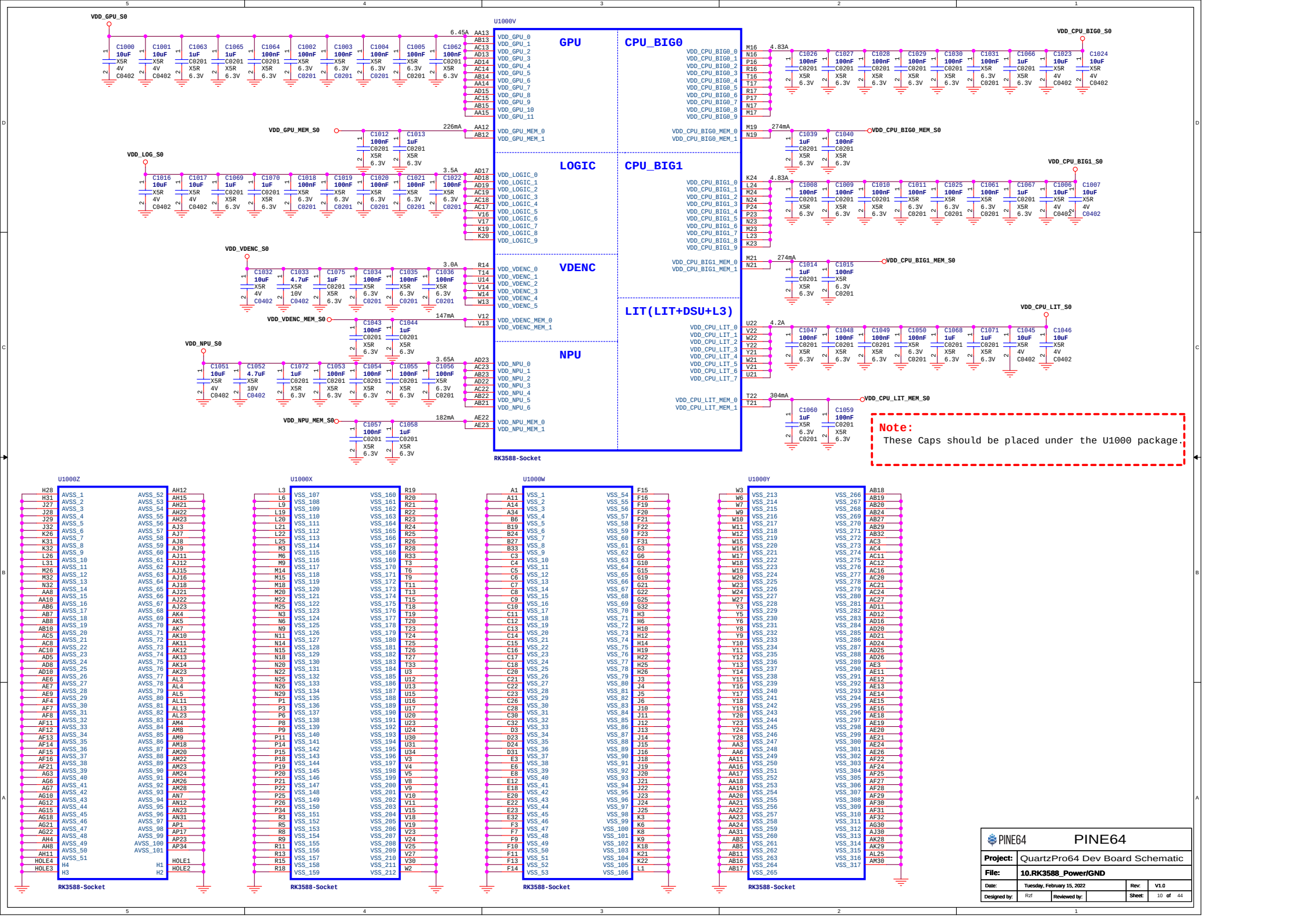
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

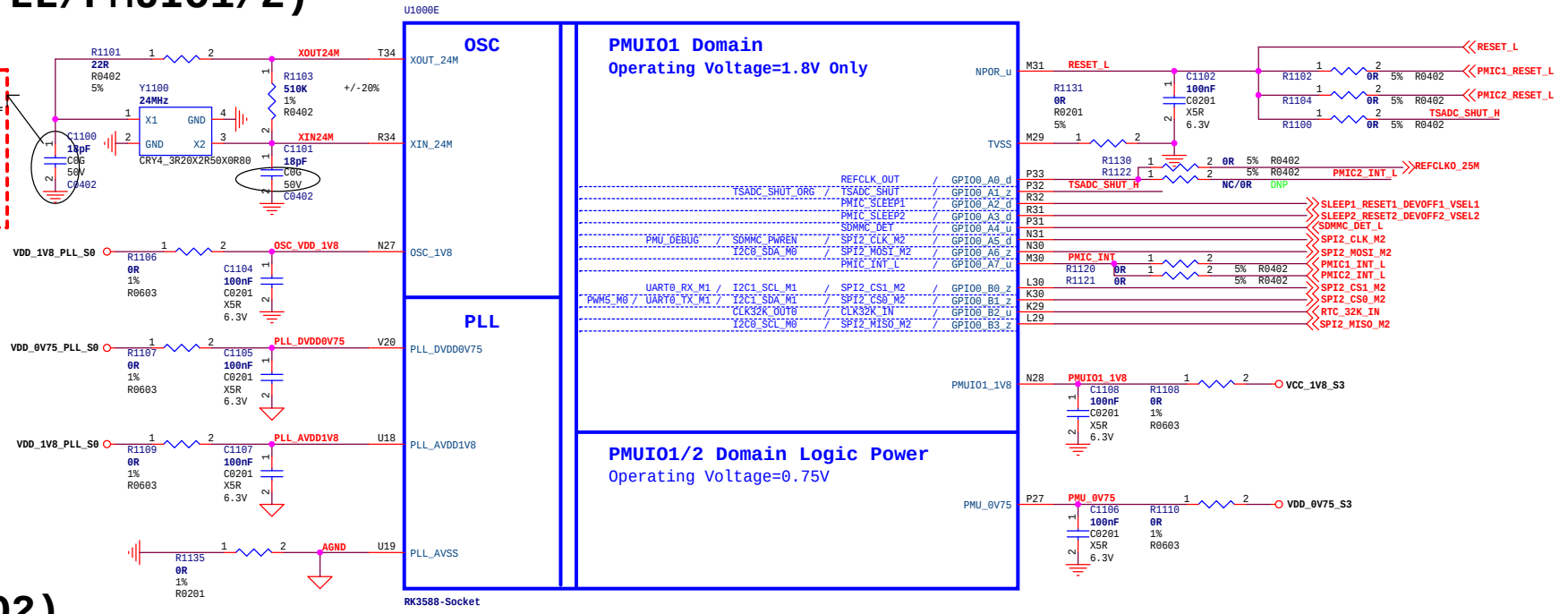
PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	08.PCIE Fun Map		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Sheet: 9 of 44


U1000V
GPU
LOGIC
VDENC
NPU
CPU_BIG0
CPU_BIG1
LIT(LIT+DSU+L3)
VDD_GPU_S0
VDD_GPU_MEM_S0
VDD_LOG_S0
VDD_VDENC_S0
VDD_VDENC_MEM_S0
VDD_NPU_S0
VDD_NPU_MEM_S0
VDD_CPU_BIG0_S0
VDD_CPU_BIG0_MEM_S0
VDD_CPU_BIG1_S0
VDD_CPU_BIG1_MEM_S0
VDD_CPU_LIT_S0
VDD_CPU_LIT_MEM_S0
RK3588-Socket
Note:
These Caps should be placed under the U1000 package.
U1000Z
U1000X
U1000W
U1000Y
PINE64
PINE64
Project: QuartzPro64 Dev Board Schematic
File: 10.RK3588_Power/GND
Date: Tuesday, February 15, 2022
Rev: V1.0
Designed by: Rzf
Reviewed by:
Sheet: 10 of 44

RK3588_E(OSC/PLL/PMUIO1/2)

Note:
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<12pF



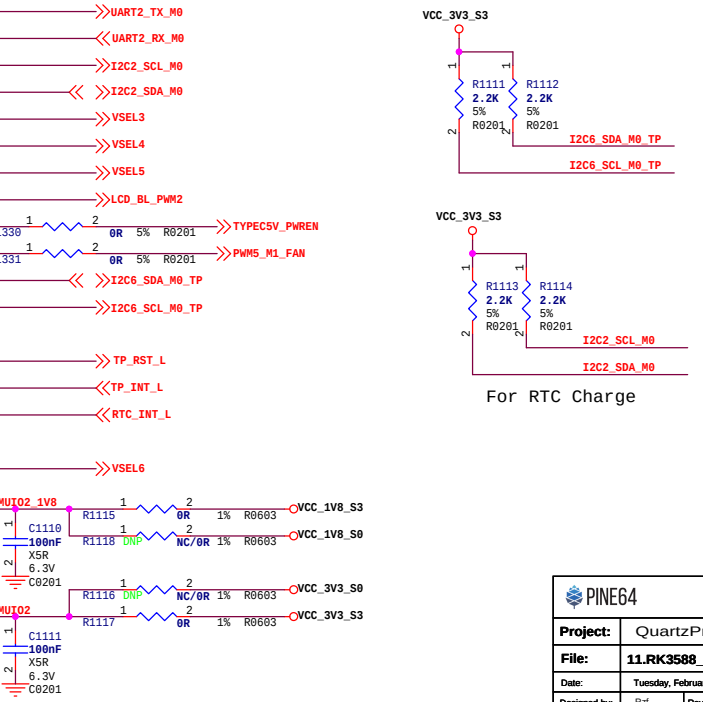
RK3588_F(PMUIO2)

U1000F

PMUIO2 Domain
Operating Voltage=1.8V/3.3V

	UART2_TX_M0			I2S1_MCLK_M1	PCIE30X1_1_CLKREQN_M0		I2C1_SCL_M0	JTAG_TCK_M2	GPIO0_B5_d
	UART2_RX_M0			I2S1_SCLK_M1	PCIE30X1_1_WAKEN_M0		I2C1_SDA_M0	JTAG_TMS_M2	GPIO0_B6_d
		CAN0_TX_M0		I2S1_LRCK_M1	PCIE30X1_1_PERSTN_M0	SPI0_CS1_M0	I2C2_SCL_M0	PWM0_M0	GPIO0_B7_d
		CAN0_RX_M0	PDM0_CLK0_M1		PCIE30X1_0_CLKREQN_M0	SPI0_MOSI_M0	I2C2_SDA_M0	PWM1_M0	GPIO0_C0_d
								PMIC_SLEEP3	GPIO0_C1_d
								PMIC_SLEEP4	GPIO0_C2_d
								PMIC_SLEEP5	GPIO0_C3_d
	UART0_RX_M0	DP0_HPDIN_M1	PDM0_CLK1_M1		PCIE30X1_0_WAKEN_M0		I2C4_SDA_M2	PWM2_M0	GPIO0_C4_d
PWM4_M0	UART0_TX_M0	DP1_HPDIN_M1		I2S1_SDI0_M1	PCIE30X1_0_PERSTN_M0		I2C4_SCL_M2	GPU_AVS	GPIO0_C5_u
PWM5_M1	UART0_RTSN	SATA_CP_POD		I2S1_SDI1_M1	PCIE30X4_CLKREQN_M0	SPI0_CLK_M0		NPU_AVS	GPIO0_C6_u
	UART1_RTSN_M2		PDM0_SDI0_M1	I2S1_SDI2_M1	PCIE30X4_WAKEN_M0	SPI0_MISO_M0	I2C6_SCL_M0	PWM6_M0	GPIO0_C7_d
	UART1_CTSN_M2		PDM0_SDI1_M1	I2S1_SDI3_M1	PCIE30X4_PERSTN_M0	SPI3_MISO_M2	I2C6_SCL_M0	PWM7_IR_M0	GPIO0_D0_d
HDMI_TX0_CEC_M1	UART1_TX_M2	UART0_CTSN	HDMI_RX_SDA_M0	I2S1_SDO0_M1	PCIE30X2_CLKREQN_M0	SPI0_CS0_M0	I2C0_SCL_M2	CPU_BIG0_AVS	GPIO0_D1_u
HDMI_TX1_CEC_M1	UART1_RX_M2		HDMI_RX_SCL_M0	I2S1_SDO1_M1	PCIE30X2_WAKEN_M0	SPI3_MOSI_M2	I2C0_SDA_M2		GPIO0_D2_u
						SPI3_CLK_M2		LITCPU_AVS	GPIO0_D3_u
HDMI_TX0_SDA_M1	SATA_CPDET	CAN2_RX_M1	PDM0_SDI2_M1	I2S1_SDO2_M1	PCIE30X2_PERSTN_M0	SPI3_CS0_M2	I2C1_SCL_M2	PWM3_IR_M0	GPIO0_D4_u
HDMI_TX0_SCL_M1	SATA_MP_SWITCH	CAN2_TX_M1		I2S1_SDO3_M1		SPI3_CS1_M2	I2C1_SDA_M2	CPU_BIG1_AVS	GPIO0_D5_u
			PDM0_SDI3_M1					PMIC_SLEEP6	GPIO0_D6_d

RK3588-Socket



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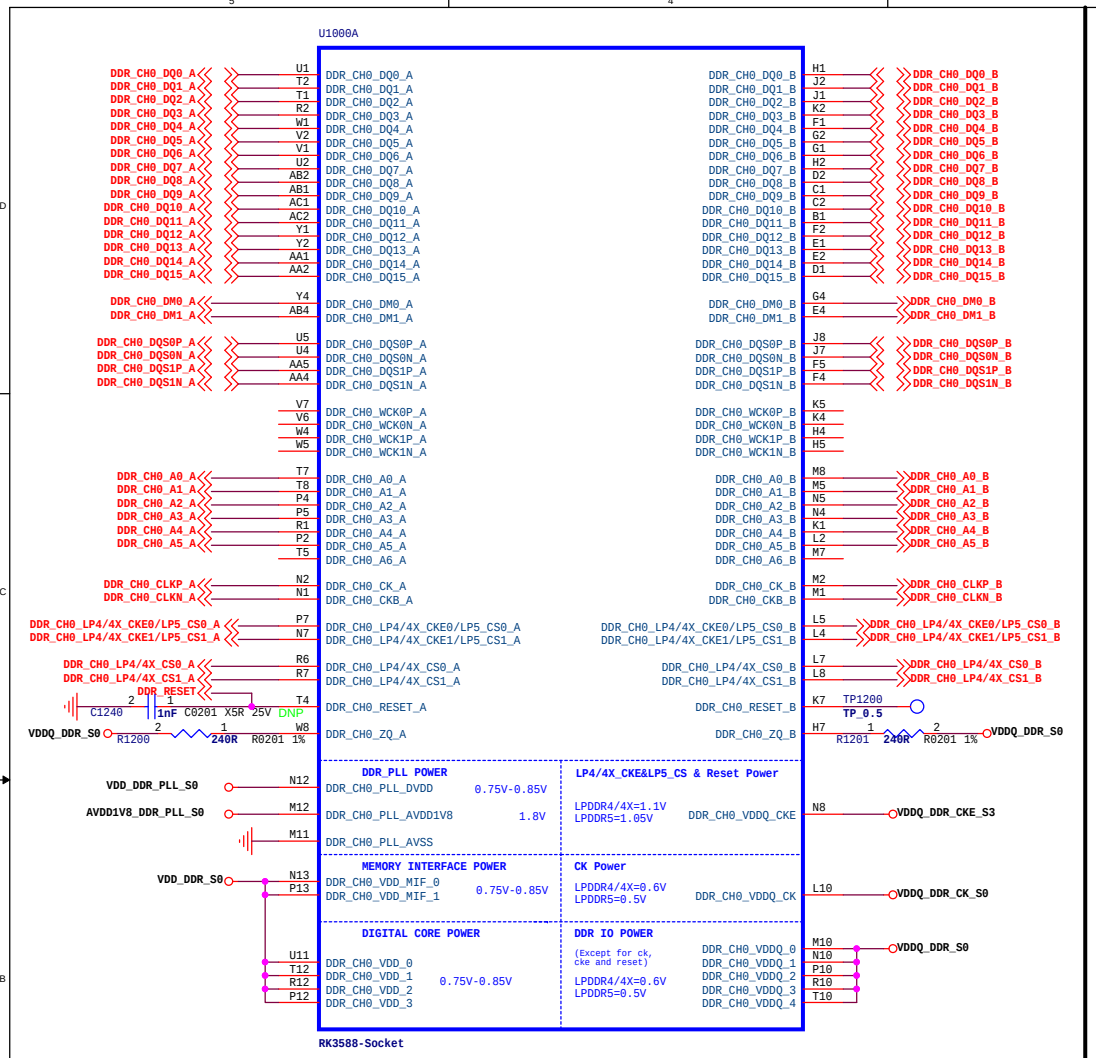
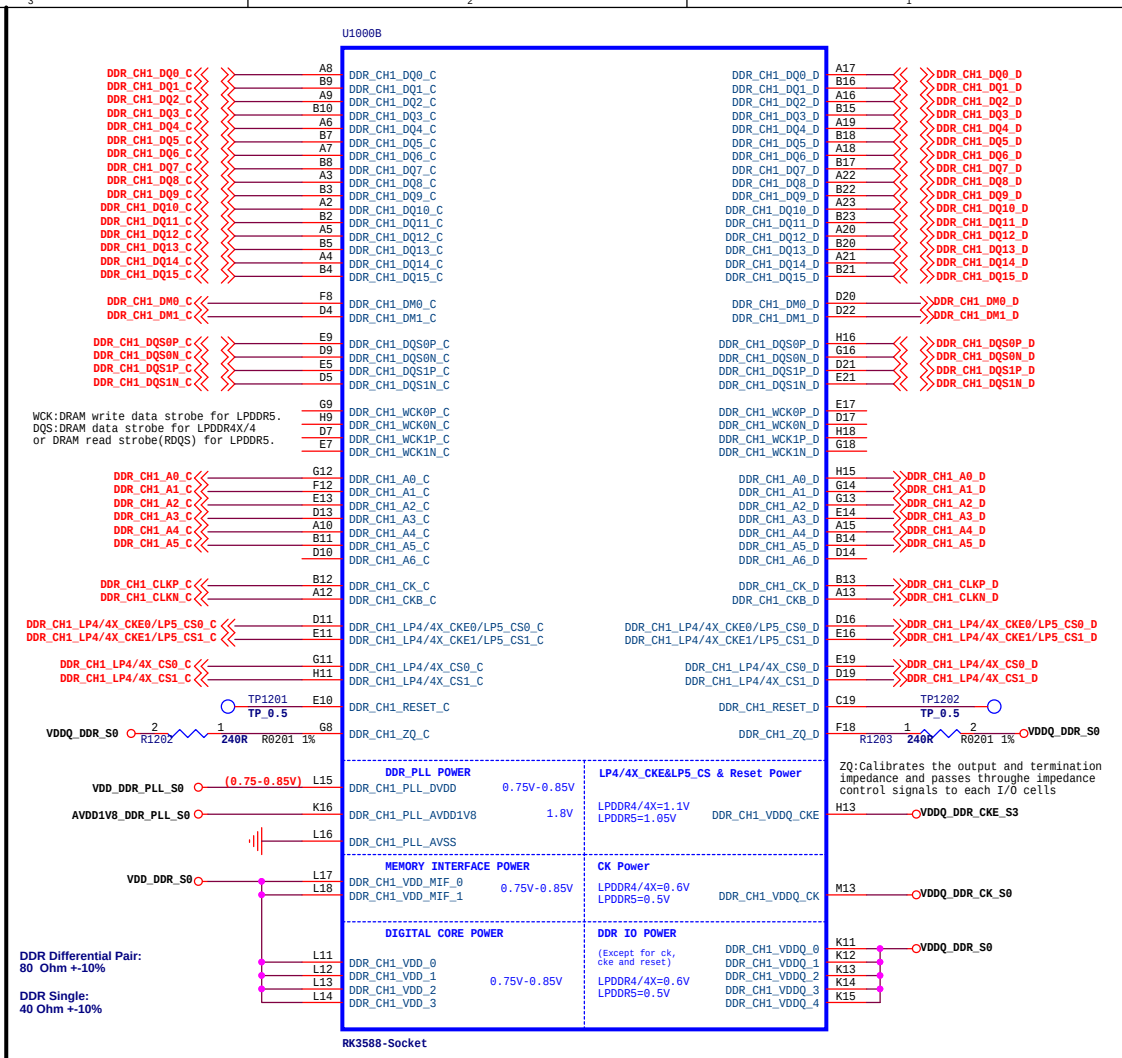
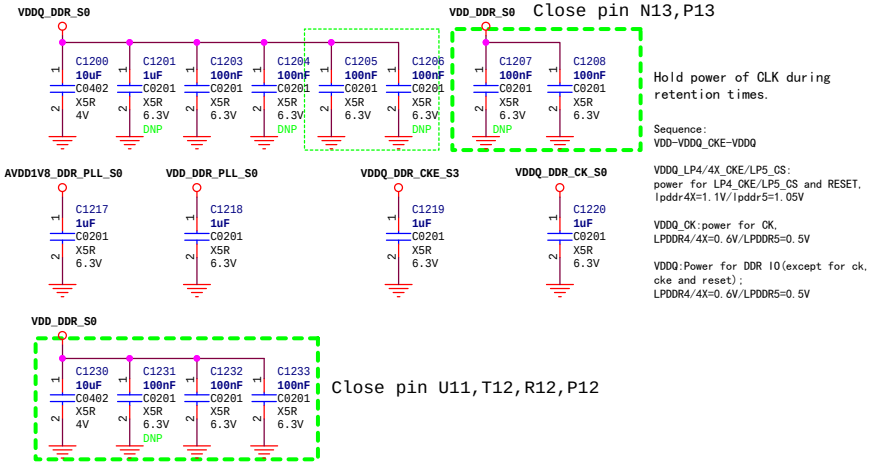
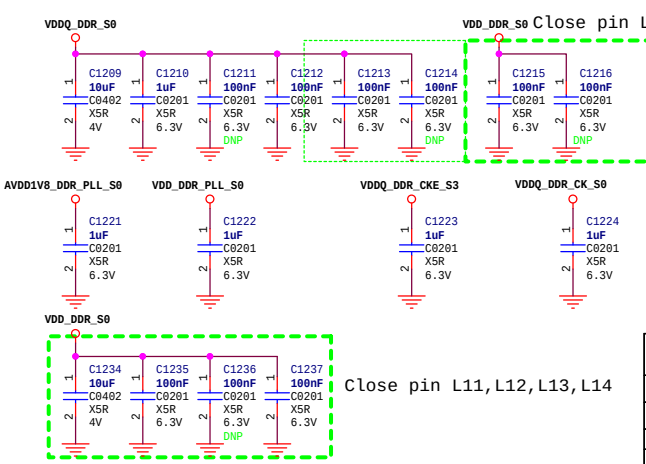
Project:	QuartzPro64 Dev Board Schematic		
File:	11.RK3588_OSC/PLL/PMUIO		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Sheet: 11 of 44





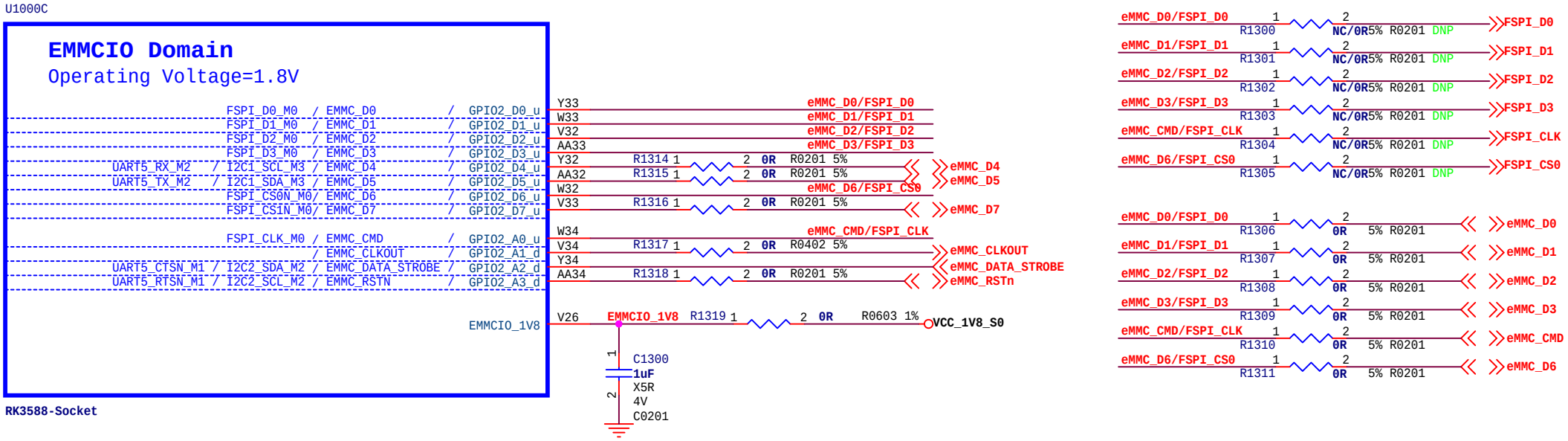
DDR FILTER



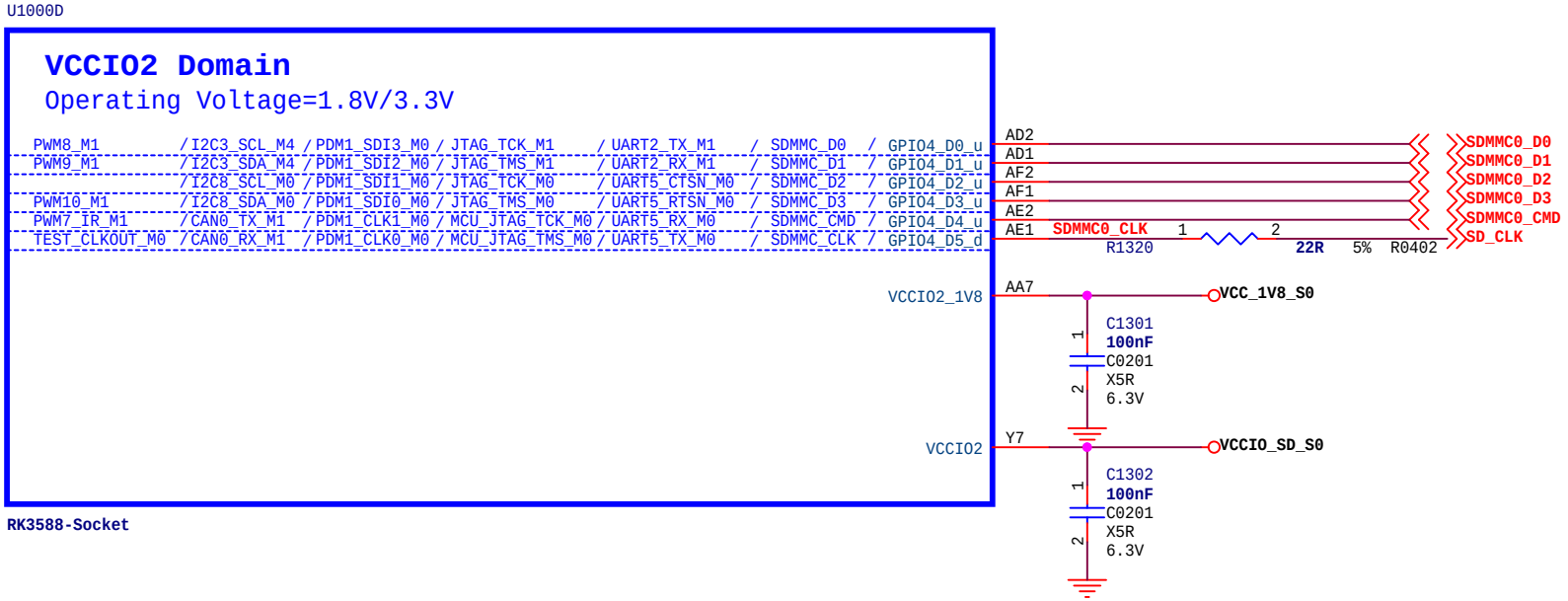


PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	12.RK3588 DDR Controler		
Date:	Monday, February 21, 2022	Rev:	V1.0
Designed by: Rzf	Reviewed by:	Sheet:	12 of 44

RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)

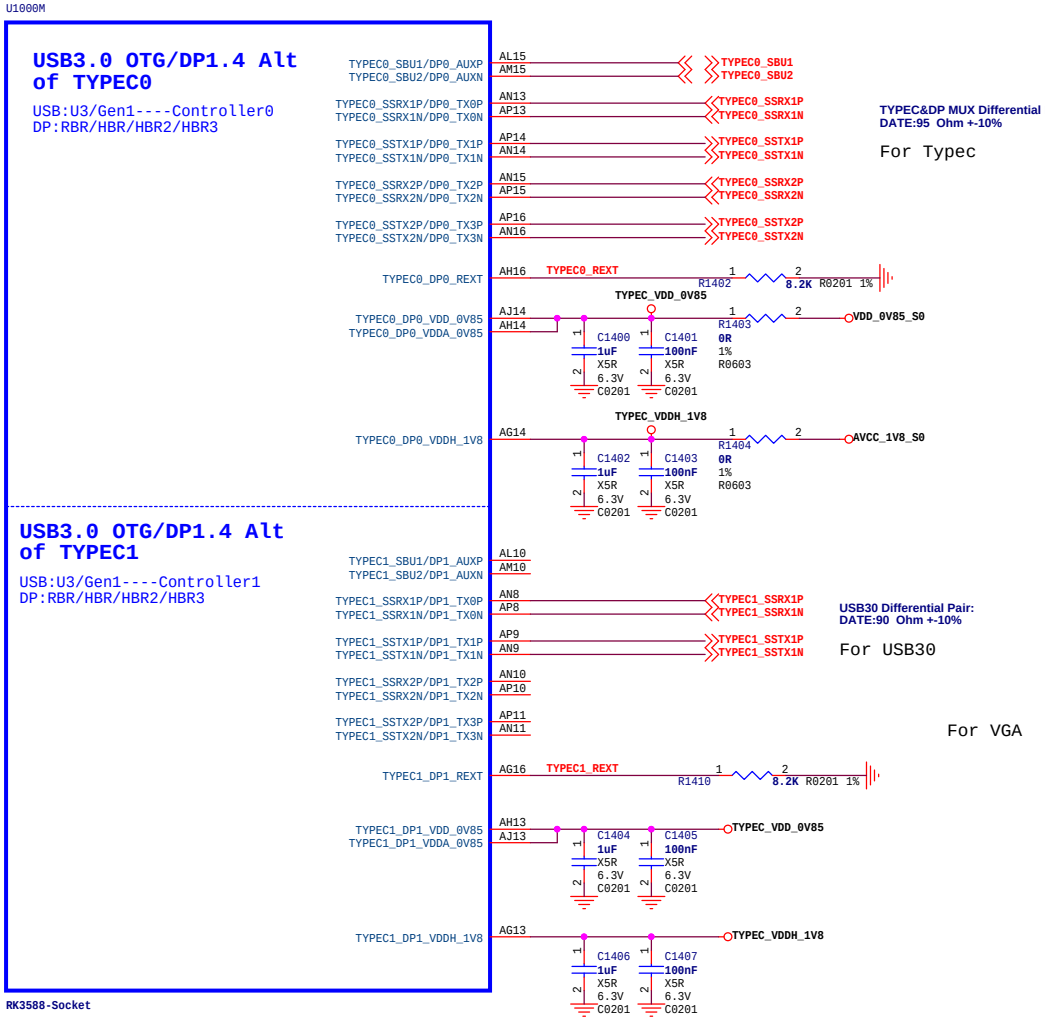


ARM JTAG(Default):
S1300:1-8,2-7 ON /3-6,4-5 OFF,

MCU JTAG:
S1300:1-8,2-7 OFF/3-6,4-5 ON,

PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**13.RK3588_Flash/SD Controller**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	13 of 44

RK3588_M(TYPEC/DP)



USB30/DP1.4 Alt Mode Configuration

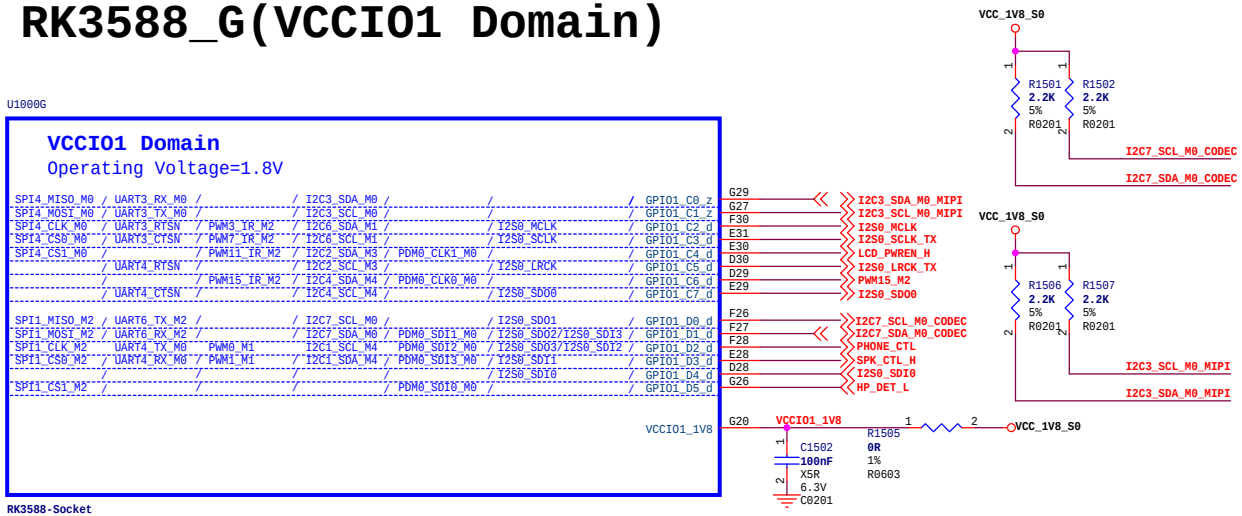
Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)

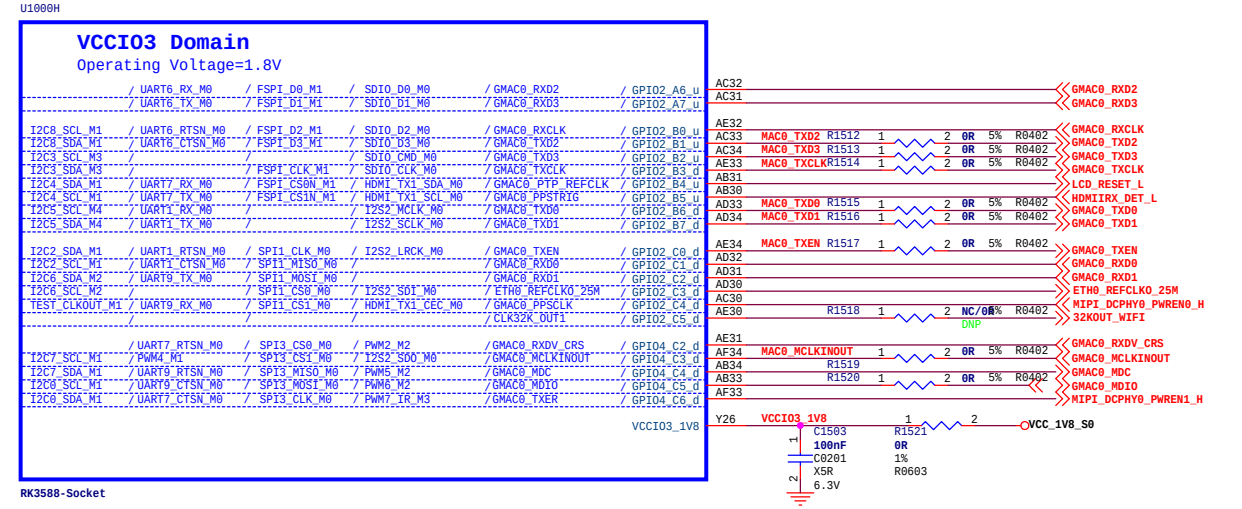
Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	14.RK3588_USB30/USB20_Ctrl				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	14 of 44

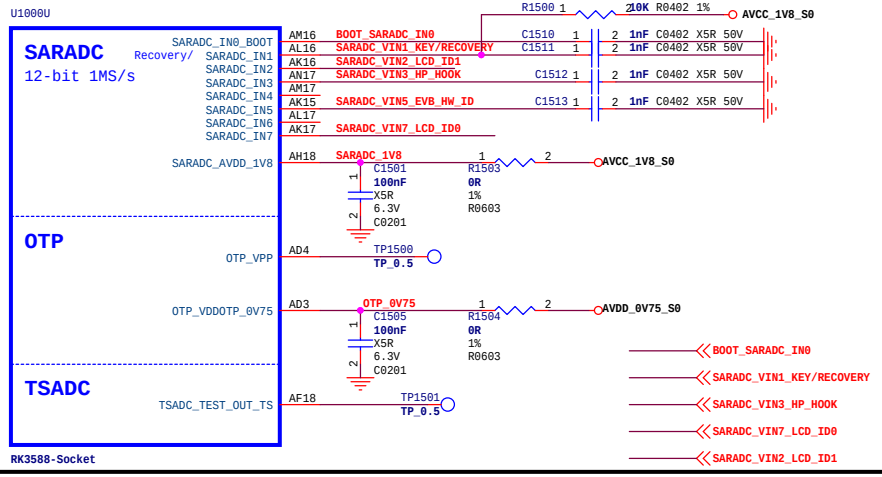
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

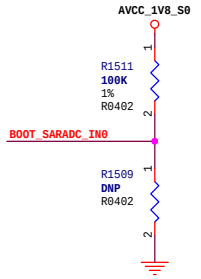
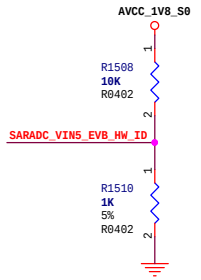


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	360K	180K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	180K	360K	2730	1.2V	FSPI M1-USB
LEVEL6	20K	100K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

TABLE 2



Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	360K	180K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	180K	360K	2730	1.2V	V5.0
LEVEL6	20K	100K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0
LEVEL8	10K	1K	380	0.16V	EVB1 V1.1

PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	15.RK3588_SARADC/1.8V Only GPIO		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by: Rzf	Reviewed by:	Sheet:	15 of 44

RK3588_Q/R(MIPI_D/C_PHY0/1)

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26 — MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B — AP26 — MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24 — MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A — AP24 — MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25 — MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C — AP25 — MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27 — MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A — AP27 — MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_D3P/NO_USE — AN28 — MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C — AP28 — MIPI_DPHY0_TX_D3N

MIPI DPHY Differential Pair:
100 Ohm +-10%

MIPI CPHY Single:
50 Ohm +-10%

MIPI D/C-PHY CSI_RX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32 — MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — AP31 — MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29 — MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — AP29 — MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30 — MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — AP30 — MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33 — MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — AP32 — MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_D3P/NO_USE — AN34 — MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — AP33 — MIPI_DPHY0_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — MIPI_D/C_PHY_VDD — C1600 2.2nF X7R 6.3V C0201
MIPI_D/C_PHY0_VDD — AG20 — R1600 NC/0R 1% R0603 DNP — AVDD_0V85_S0
C1602 100nF X5R 6.3V C0201; C1601 1uF X5R 6.3V C0201; R1602 0R 1% R0603 — AVDD_0V75_S0
D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V
MIPI_D/C_PHY_VDD1V2
MIPI_D/C_PHY0_VDD_1V2 — AH20 — R1604 0R 1% R0603 — AVDD_1V2_S0
C1603 1uF X5R 6.3V C0201; C1604 100nF X5R 6.3V C0201
MIPI_D/C_PHY_VDD1V8
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — R1606 0R 1% R0603 — AVCC_1V8_S0
C1605 1uF X5R 6.3V C0201; C1606 100nF X5R 6.3V C0201

RK3588-Socket

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20 — MIPI_DPHY1_TX_CLKP
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — AP20 — MIPI_DPHY1_TX_CLKN
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18 — MIPI_DPHY1_TX_D0P
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — AP18 — MIPI_DPHY1_TX_D0N
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19 — MIPI_DPHY1_TX_D1P
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — AP19 — MIPI_DPHY1_TX_D1N
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21 — MIPI_DPHY1_TX_D2P
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A — AP21 — MIPI_DPHY1_TX_D2N
MIPI_DPHY1_TX_D3P/NO_USE — AN22 — MIPI_DPHY1_TX_D3P
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C — AP22 — MIPI_DPHY1_TX_D3N

MIPI D/C-PHY CSI_RX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20 — MIPI_DPHY1_RX_CLKP
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B — AL20 — MIPI_DPHY1_RX_CLKN
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18 — MIPI_DPHY1_RX_D0P
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A — AL18 — MIPI_DPHY1_RX_D0N
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19 — MIPI_DPHY1_RX_D1P
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C — AL19 — MIPI_DPHY1_RX_D1N
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21 — MIPI_DPHY1_RX_D2P
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A — AL21 — MIPI_DPHY1_RX_D2N
MIPI_DPHY1_RX_D3P/NO_USE — AK22 — MIPI_DPHY1_RX_D3P
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C — AL22 — MIPI_DPHY1_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C1608 2.2nF X7R 6.3V C0201
MIPI_D/C_PHY1_VDD — AG19 — MIPI_D/C_PHY_VDD — C1609 1uF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V2 — AH19 — MIPI_D/C_PHY_VDD1V2 — C1611 100nF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — MIPI_D/C_PHY_VDD1V8 — C1613 1uF X5R 6.3V C0201

RK3588-Socket

Note:
These Caps should be placed under the U1000 package.

RK3588_P(MIPI_CSI_RX_PHY)

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P — AJ33 — MIPI_CSI0_RX_CLK0P
MIPI_CSI0_CLK0N — AJ34 — MIPI_CSI0_RX_CLK0N
MIPI_CSI0_D0P — AG33 — MIPI_CSI0_RX_D0P
MIPI_CSI0_D0N — AG34 — MIPI_CSI0_RX_D0N
MIPI_CSI0_D1P — AH33 — MIPI_CSI0_RX_D1P
MIPI_CSI0_D1N — AH34 — MIPI_CSI0_RX_D1N
MIPI_CSI0_CLK1P — AM33 — MIPI_CSI0_RX_CLK1P
MIPI_CSI0_CLK1N — AM34 — MIPI_CSI0_RX_CLK1N
MIPI_CSI0_D2P — AK33 — MIPI_CSI0_RX_D2P
MIPI_CSI0_D2N — AK34 — MIPI_CSI0_RX_D2N
MIPI_CSI0_D3P — AL33 — MIPI_CSI0_RX_D3P
MIPI_CSI0_D3N — AL34 — MIPI_CSI0_RX_D3N

MIPI CSI Differential Pair:
100 Ohm +-10%

MIPI_CSI_AVCC0V75
MIPI_CSI0_AVCC0V75 — AB25 — R1608 0R 1% R0603 — AVDD_0V75_S0
C1615 1uF X5R 6.3V C0201; C1616 100nF X5R 6.3V C0201
MIPI_CSI_AVCC1V8
MIPI_CSI0_AVCC1V8 — AB26 — R1609 0R 1% R0603 — AVCC_1V8_S0
C1617 1uF X5R 6.3V C0201; C1618 100nF X5R 6.3V C0201

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P — AJ31 — MIPI_CSI1_RX_CLK0P
MIPI_CSI1_CLK0N — AJ32 — MIPI_CSI1_RX_CLK0N
MIPI_CSI1_D0P — AG31 — MIPI_CSI1_RX_D0P
MIPI_CSI1_D0N — AG32 — MIPI_CSI1_RX_D0N
MIPI_CSI1_D1P — AH31 — MIPI_CSI1_RX_D1P
MIPI_CSI1_D1N — AH32 — MIPI_CSI1_RX_D1N
MIPI_CSI1_CLK1P — AM31 — MIPI_CSI1_RX_CLK1P
MIPI_CSI1_CLK1N — AM32 — MIPI_CSI1_RX_CLK1N
MIPI_CSI1_D2P — AK31 — MIPI_CSI1_RX_D2P
MIPI_CSI1_D2N — AK32 — MIPI_CSI1_RX_D2N
MIPI_CSI1_D3P — AL31 — MIPI_CSI1_RX_D3P
MIPI_CSI1_D3N — AL32 — MIPI_CSI1_RX_D3N

MIPI_CSI1_AVCC0V75 — AA25 — MIPI_CSI_AVCC0V75 — C1619 1uF X5R 6.3V C0201
MIPI_CSI1_AVCC1V8 — AA26 — MIPI_CSI_AVCC1V8 — C1621 100nF X5R 6.3V C0201

RK3588-Socket

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

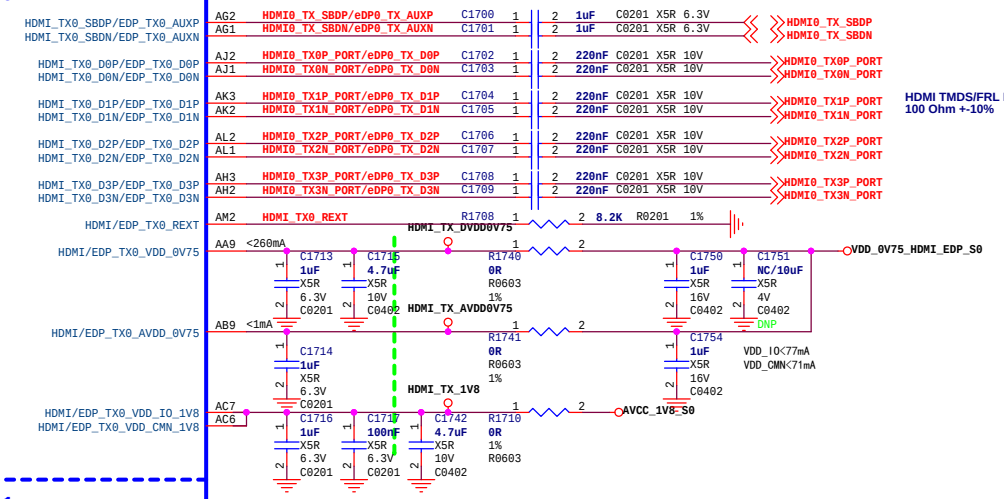
PINE64	PINE64
Project:	QuartzPro64 Dev Board Schematic
File:	16.RK3588_MIPI Interface
Date:	Tuesday, February 15, 2022
Rev:	V1.0
Designed by:	Rzf
Reviewed by:	
Sheet:	16 of 44

RK3588_S(HDMI2.1 TX)

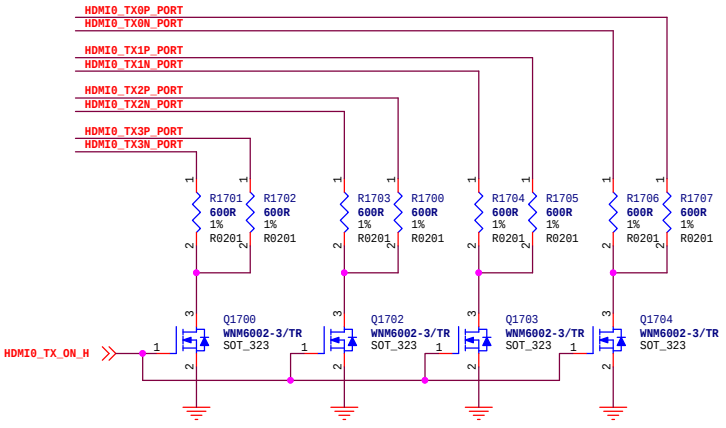
U1000S

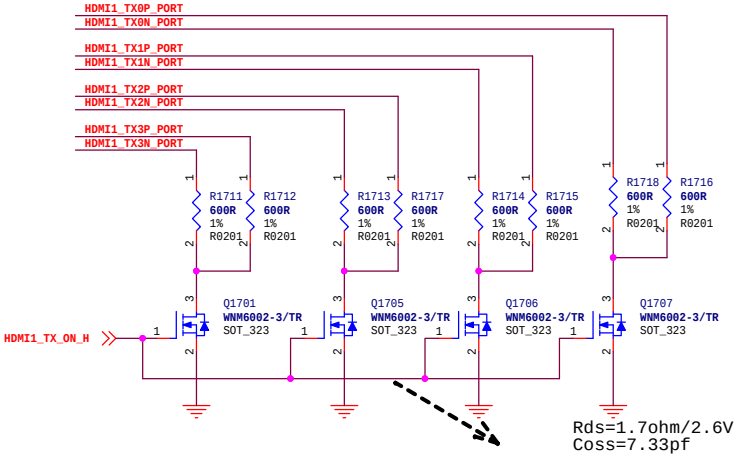
HDMI TX/eDP MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps



HDMI TMDS/FRL Pair
100 Ohm +-10%

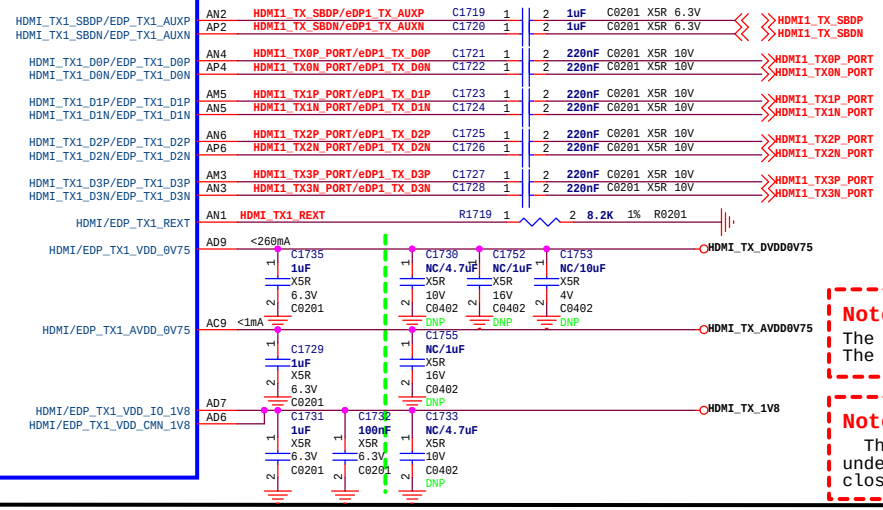




Rds=1.7ohm/2.6V
Coss=7.33pf

HDMI TX/eDP MUX Port1

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps



RK3588-Socket

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

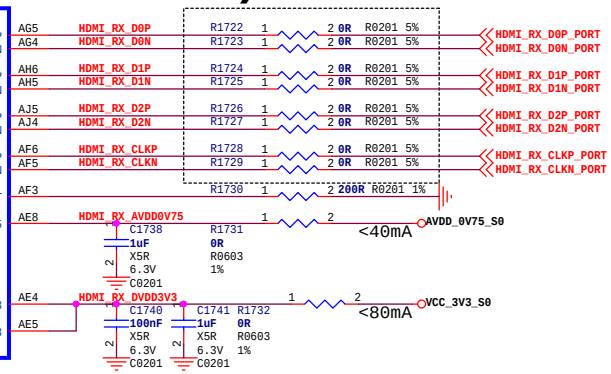
RK3588_T(HDMI20 RX)

U1000T

Place close HDMI port.

HDMI RX

HDMI:V2.0



HDMI20_RX
100 Ohm +-10%

RK3588-Socket

PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	17.RK3588_HDMI/eDP Interface		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Sheet: 17 of 44

RK3588_N(PCIE20)

CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

input or output

PCIE20_0_REFCLKP
PCIE20_0_REFCLKN
PCIE20_0_TXP/SATA30_0_TXP
PCIE20_0_TXN/SATA30_0_TXN
PCIE20_0_RXP/SATA30_0_RXP
PCIE20_0_RXN/SATA30_0_RXN
PCIE20_SATA30_0_AVDD_0V85
PCIE20_SATA30_0_AVDD_1V8

L32 L33 → PCIE20_0_REFCLKP / PCIE20_0_REFCLKN
M34 M33 → C1822 C1823 10nF C0201 X5R 10V → SATA30_0_TXP / SATA30_0_TXN
N33 N34 → SATA30_0_RXP / SATA30_0_RXN
M28 → PCIE20_AVDD0V85: C1810 100nF X5R 6.3V C0201; C1811 4.7uF X5R 10V C0402
M27 → PCIE20_AVDD1V8: C1808 100nF X5R 6.3V C0201; C1809 4.7uF X5R 10V C0402

For WIFI

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

input or output

PCIE20_1_REFCLKP
PCIE20_1_REFCLKN
PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN
PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN
PCIE20_SATA30_1_AVDD_0V85
PCIE20_SATA30_1_AVDD_1V8

H32 H33 → PCIE20_1_REFCLKP / PCIE20_1_REFCLKN
K33 PCIE20_1_TXP — C1824 — 100nF X5R 6.3VC0201 → PCIE20_1_TXP/SATA30_1_TXP
K34 PCIE20_1_TXN — C1825 — 100nF X5R 6.3VC0201 → PCIE20_1_TXN/SATA30_1_TXN
J33 J34 → PCIE20_1_RXP/SATA30_1_RXP / PCIE20_1_RXN/SATA30_1_RXN
L28 → PCIE20_AVDD0V85: C1818 100nF X5R 6.3V C0201; C1819 4.7uF X5R 10V C0402
L27 → PCIE20_AVDD1V8: C1816 100nF X5R 6.3V C0201; C1817 4.7uF X5R 10V C0402

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 HOST
Controller2

MUX

input or output

PCIE20_2_REFCLKP
PCIE20_2_REFCLKN
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN
PCIE20_SATA30_USB30_2_AVDD_0V85
PCIE20_SATA30_USB30_2_AVDD_1V8

G31 G30 → PCIE20_2_REFCLKP / PCIE20_2_REFCLKN
H30 H29 → C1820 C1821 100nF C0201 X5R 6.3V → PCIE20_2_TXP / PCIE20_2_TXN
J31 J30 → PCIE20_2_RXP / PCIE20_2_RXN
PCIE20_AVDD0V85
K28 → AVDD_0V85_S0: C1806 100nF X5R 6.3V C0201; C1807 4.7uF X5R 10V C0402; R1800 0R 1% R0603
PCIE20_AVDD1V8
K27 → AVCC_1V8_S0: C1804 1uF X5R 6.3V C0201; C1805 4.7uF X5R 10V C0402; R1803 0R 1% R0603

For RJ45

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588-Socket

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

RK3588_O(PCIE30)

Note:
Only PCIE30 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE20/SATA30 MUX1

PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input
PCIE30_PORT0_REF_CLKP
PCIE30_PORT0_REF_CLKN

Lane0
PCIE30_PORT0_TX0P
PCIE30_PORT0_TX0N
PCIE30_PORT0_RX0P
PCIE30_PORT0_RX0N

Lane1
PCIE30_PORT0_TX1P
PCIE30_PORT0_TX1N
PCIE30_PORT0_RX1P
PCIE30_PORT0_RX1N

PCIE30_PORT0_RESREF
PCIE30_PORT0_AVDD0V75
PCIE30_PORT0_AVDD1V8

E33 E34 → PCIE30_PORT0_REFCLKP_IN / PCIE30_PORT0_REFCLKN_IN
D32 D33 → PCIE30_PORT0_TX0P / PCIE30_PORT0_TX0N
G33 G34 → PCIE30_PORT0_RX0P / PCIE30_PORT0_RX0N
C33 C34 → PCIE30_PORT0_TX1P / PCIE30_PORT0_TX1N
F32 F33 → PCIE30_PORT0_RX1P / PCIE30_PORT0_RX1N
B34 PCIE30_0_REF — R1801 200R 1% R0201
PCIE30_AVDD_0V75
G24 → AVDD_0V75_S0: C1802 1uF X5R 6.3V C0201; C1803 4.7uF X5R 10V C0402; R1802 0R 1% R0603
PCIE30_AVDD_1V8
G23 → AVCC_1V8_S0: C1800 1uF X5R 6.3V C0201; C1801 4.7uF X5R 10V C0402; R1804 0R 1% R0603

CLK Differential Pair:
100 Ohm ±10%
DATA Differential Pair:
PCIE30: 85 Ohm ±10%

PCIE30 PORT1

input
PCIE30_PORT1_REF_CLKP
PCIE30_PORT1_REF_CLKN

Lane0
PCIE30_PORT1_TX0P
PCIE30_PORT1_TX0N
PCIE30_PORT1_RX0P
PCIE30_PORT1_RX0N

Lane1
PCIE30_PORT1_TX1P
PCIE30_PORT1_TX1N
PCIE30_PORT1_RX1P
PCIE30_PORT1_RX1N

PCIE30_PORT1_RESREF
PCIE30_PORT1_AVDD0V75
PCIE30_PORT1_AVDD1V8

A28 B28 → PCIE30_PORT1_REFCLKP_IN / PCIE30_PORT1_REFCLKN_IN
B30 A30 → PCIE30_PORT1_TX2P / PCIE30_PORT1_TX2N
B32 A32 → PCIE30_PORT1_RX2P / PCIE30_PORT1_RX2N
C29 B29 → PCIE30_PORT1_TX3P / PCIE30_PORT1_TX3N
C31 B31 → PCIE30_PORT1_RX3P / PCIE30_PORT1_RX3N
A33 PCIE30_1_REF — R1807 200R 1% R0201
H24 → PCIE30_AVDD_0V75: C1814 1uF X5R 6.3V C0201; C1815 4.7uF X5R C0402 10V
H23 → PCIE30_AVDD_1V8: C1812 100nF X5R 6.3V C0201; C1813 4.7uF X5R 10V C0402

RK3588-Socket

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	18.RK3588_PCIE30/PCIE20/SATA30				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	18 of 44

RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

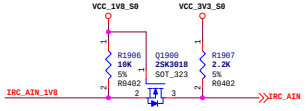
Operating Voltage=1.8V/3.3V

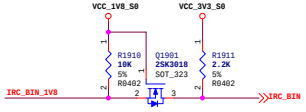
PWM10_M0	/ SPI4_MISO_M1	/	/ I2C6_SDA_M4	/FSPI_D0_M2	/I2S3_MCLK	/ SDIO_D0_M1	/GMAC1_TXD2	/ GPIO3_A0_u	AA29 BT_WAKE_HOST_H
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/I2C6_SCL_M4	/FSPI_D1_M2	/I2S3_SCLK	/ SDIO_D1_M1	/GMAC1_TXD3	/ GPIO3_A1_u	AA30 HOST_WAKE_BT_H
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_TX_M1	/	/FSPI_D2_M2	/I2S3_LRCK	/ SDIO_D2_M1	/GMAC1_RXD2	/ GPIO3_A2_u	AD27 UART8_TX_M1_BT
AUDDSM_RN	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/FSPI_D3_M2	/I2S3_SDO	/ SDIO_D3_M1	/GMAC1_RXD3	/ GPIO3_A3_u	AE27 UART8_RX_M1_BT
AUDDSM_RP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/		/I2S3_SDI	/ SDIO_CMD_M1	/ GMAC1_TXCLK	/ GPIO3_A4_d	AD28 UART8_RTSn_M1_BT
	/ MIPI_CAMERA0_CLK_M1	/ UART8_CTSN_M1	/ I2C4_SDA_M0	/FSPI_CLK_M2	/	/ SDIO_CLK_M1	/ GMAC1_RXCLK	/ GPIO3_A5_d	AH30 UART8_CTSn_M1_BT
	/ MIPI_CAMERA1_CLK_M1	/	/ I2C4_SCL_M0	/	/	/	/ ETH1_REFCLKO_25M	/ GPIO3_A6_d	AH27 BT_REG_ON_H
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/ GMAC1_RXD0	/ GPIO3_A7_u	AG29 WIFI_WAKE_HOST_H
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/	/	/ GMAC1_RXD1	/ GPIO3_B0_u	AG28 PCIE30X4_PRSNT_L
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART2_TX_M2	/	/	/	/	/ GMAC1_RXDV_CRS	/ GPIO3_B1_d	AH29 WIFI_REG_ON_H
PWM3_IR_M1	/	/ UART2_RX_M2	/	/	/I2S2_SDI_M1	/	/ GMAC1_TXER	/ GPIO3_B2_d	AE28 I2S2_SDI_M1_BT
	/	/ UART2_RTSN	/	/	/I2S2_SDO_M1	/	/ GMAC1_TXD0	/ GPIO3_B3_u	AC28 I2S2_SDO_M1_BT
	/	/ UART2_CTSN	/	/	/I2S2_MCLK_M1	/	/ GMAC1_TXD1	/ GPIO3_B4_u	AC29 CC_INT_L
PWM12_M0	/ CAN1_RX_M0	/ UART3_TX_M1	/	/	/I2S2_SCLK_M1	/	/ GMAC1_TXEN	/ GPIO3_B5_u	AD29 I2S2_SCLK_TX_M1_BT
PWM13_M0	/ CAN1_TX_M0	/ UART3_RX_M1	/	/	/I2S2_LRCK_M1	/	/ GMAC1_MCLKINOUT	/ GPIO3_B6_d	AE29 I2S2_LRCK_TX_M1_BT
	/	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/HDMI_TX1_HPD_M1	/	/ GMAC1_PTP_REF_CLK	/ GPIO3_B7_d	AA28 Power_LED_EN_H
	/	/ UART7_TX_M1	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/	/ GMAC1_PPSTRIG	/ GPIO3_C0_d	Y29 IRC_AIN_1V8
	/ PCIE30X2_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/ GMAC1_PPSCLK	/ GPIO3_C1_d	Y27 IRC_BIN_1V8
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C8_SCL_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GMAC1_MDC	/ GPIO3_C2_d	Y31 MIPI_TE0/PWM14_M0_1V8
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GMAC1_MDIO	/ GPIO3_C3_d	Y30 PCIE30x4_PWREN_H
CAN2_RX_M0	/ PCIE30X4_CLKREQN_M2	/ UART5_TX_M1	/ FSPI_CS0N_M2	/ SPI3_CS0_M3	/HDMI_TX1_CEC_M2	/	/ CIF_D8	/ GPIO3_C4_u	AH26 HDMITX1_CEC_M2
CAN2_TX_M0	/ PCIE30X4_WAKEN_M2	/ UART5_RX_M1	/ FSPI_CS1N_M2	/ SPI3_CS1_M3	/HDMI_TX1_SDA_M1	/	/ CIF_D9	/ GPIO3_C5_u	AH25 HDMITX1_SDA_M1
	/ PCIE30X4_PERSTN_M2	/	/	/ SPI3_MISO_M3	/HDMI_TX1_SCL_M1	/	/ CIF_D10	/ GPIO3_C6_u	AG26 HDMITX1_SCL_M1
	/ PCIE20X1_2_CLKREQN_M0	/	/ I2C5_SCL_M0	/ SPI3_MOSI_M3	/HDMI_TX0_SCL_M2	/	/ CIF_D11	/ GPIO3_C7_u	AJ24 I2C5_SCL_M0_MIPI
PWM8_M2	/ PCIE20X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C5_SDA_M0	/ SPI3_CLK_M3	/HDMI_TX0_SDA_M2	/	/ CIF_D12	/ GPIO3_D0_u	AH24 I2C5_SDA_M0_MIPI
PWM9_M2	/ PCIE20X1_2_PERSTN_M0	/ UART4_TX_M1	/	/ SPI0_MISO_M3	/HDMI_RX_CEC_M1	/	/ CIF_D13	/ GPIO3_D1_d	AG23 HDMI_RX_CEC
	/ PCIE30X2_CLKREQN_M2	/ UART9_RTSN_M2	/ I2C7_SCL_M2	/ SPI0_MOSI_M3	/HDMI_RX_SCL_M1	/	/ CIF_D14	/ GPIO3_D2_d	AG25 HDMI_RX_SCL_M1
PWM10_M2	/ PCIE30X2_WAKEN_M2	/ UART9_CTSN_M2	/ I2C7_SDA_M2	/ SPI0_CLK_M3	/HDMI_RX_SDA_M1	/	/ CIF_D15	/ GPIO3_D3_u	AG24 HDMI_RX_SDA_M1
	/ PCIE30X2_PERSTN_M2	/ UART9_RX_M2	/	/ SPI0_CS0_M3	/HDMI_RX_HPDOUT_M1	/ HDMI_TX0_HPD_M1	/ MCU_JTAG_TCK_M1	/ GPIO3_D4_d	AA27 HDMIIRX_HPDOUT_H
PWM11_IR_M3	/ PCIE30X4_BUTTON_RSTN	/ UART9_TX_M2	/	/ SPI0_CS1_M3	/DP1_HPDIN_M0	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D5_d	AB28

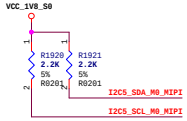
VCCIO5_1V8 — W25 VDDIO5_1V8 — C1903 100nF X5R 6.3V C0201 — R1902 0R 1% R0603 — 1 — 2 — VCC_1V8_S0

VCCIO5 — W26 — C1902 100nF X5R 6.3V C0201

RK3588-Socket







RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

		/ SPI0_MISO_M1	/ UART9_RTSN_M1 /		/ I2S1_MCLK_M0	/ PCIE30X1_1_CLKREQN_M1	/ BT1120_D0	/ CIF_D0	/ GPIO4_A0_d AK30 PCIEX1_1_CLKREQn_M1_L
		/ SPI0_MOSI_M1	/ UART9_CTSN_M1 /		/ I2S1_SCLK_M0	/ PCIE30X1_1_WAKEN_M1	/ BT1120_D1	/ CIF_D1	/ GPIO4_A1_d AL30 PCIEX1_1_WAKEn_M1_L
		/ SPI0_CLK_M1	/	/	/ I2S1_LRCK_M0	/ PCIE30X1_1_PERSTN_M1	/ BT1120_D2	/ CIF_D2	/ GPIO4_A2_d AM29 PCIEX1_1_PERSTn_M1_L
		/	UART0_TX_M2	/	/	/ PCIE30X1_0_CLKREQN_M1	/ BT1120_D3	/ CIF_D3	/ GPIO4_A3_d AL29 PCIEX1_0_CLKREQn_M1_L
		/ SPI2_MISO_M1	/ UART0_RX_M2	/ I2C3_SCL_M2	/	/ PCIE30X1_0_WAKEN_M1	/ BT1120_D4	/ CIF_D4	/ GPIO4_A4_d AL28 PCIEX1_0_WAKEn_M1_L
		/ SPI2_MOSI_M1	/ UART3_TX_M2	/ I2C3_SDA_M2	/ I2S1_SDI0_M0	/ PCIE30X1_0_PERSTN_M1	/ BT1120_D5	/ CIF_D5	/ GPIO4_A5_d AK27 PCIEX1_0_PERSTn_M1_L
		/ SPI2_CLK_M1	/ UART3_RX_M2	/ I2C5_SCL_M2	/ I2S1_SDI1_M0	/ PCIE30X2_CLKREQN_M1	/ BT1120_D6	/ CIF_D6	/ GPIO4_A6_d AL27 TYPEC0_SBU1_DC
		/ SPI2_CS0_M1	/	/ I2C5_SDA_M2	/ I2S1_SDI2_M0	/ PCIE30X2_WAKEN_M1	/ BT1120_D7	/ CIF_D7	/ GPIO4_A7_d AM27 TYPEC0_SBU2_DC
		/ SPI2_CS1_M1	/ UART8_TX_M0	/ I2C6_SDA_M3	/ I2S1_SDI3_M0	/ PCIE30X2_PERSTN_M1	/ BT1120_CLKOUT	/ CIF_CLKIN	/ GPIO4_B0_d AK26 USB_HOST_PWREN_H
SATA2_ACT_LED_M0	/ SPDIF1_TX_M1	/ SPI0_CS1_M1	/ UART8_RX_M0	/ I2C6_SCL_M3	/ I2S1_SDO0_M0	/ PCIE30X1_0_BUTTON_RSTN	/	/ MIPI_CAMERA0_CLK_M0	/ GPIO4_B1_u AL24 HDMI0_TX_ON_H
CAN1_RX_M1	/ PWM14_M1	/ SPI0_CS0_M1	/ UART8_RTSN_M0	/ I2C7_SCL_M3	/ I2S1_SDO1_M0	/ PCIE30X1_1_BUTTON_RSTN	/ BT1120_D8	/ CIF_HREF	/ GPIO4_B2_u AK25 HDMI1_TX_ON_H
CAN1_TX_M1	/ PWM15_IR_M1	/	/ UART8_CTSN_M0	/ I2C7_SDA_M3	/ I2S1_SDO2_M0	/ PCIE20X1_2_BUTTON_RSTN	/ BT1120_D9	/ CIF_VSYNC	/ GPIO4_B3_u AM25 GMAC0_RSTn_L
SPDIF0_TX_M1	/ PWM11_IR_M1	/ DP0_HPDIN_M0	/ UART9_TX_M1	/	/ I2S1_SDO3_M0	/ PCIE30X4_CLKREQN_M1	/ BT1120_D10	/ CIF_CLKOUT	/ GPIO4_B4_u AL26 PCIE30X4_CLKREQn_M1_L
SATA1_ACT_LED_M0	/ PWM12_M1	/ SPI3_MISO_M1	/ UART9_RX_M1	/	/ HDMI_RX_CEC_M0	/ PCIE30X4_WAKEN_M1	/ BT1120_D11	/	/ GPIO4_B5_d AJ26 PCIE30X4_WAKEn_M1_L
SATA0_ACT_LED_M0	/ PWM13_M1	/ SPI3_MOSI_M1	/	/ I2C5_SCL_M1	/ HDMI_RX_HPDOUT_M0	/ PCIE30X4_PERSTN_M1	/ BT1120_D12	/	/ GPIO4_B6_d AJ27 PCIE30X4_PERSTn_M1_L
	/	/ SPI3_CLK_M1	/	/ I2C5_SDA_M1	/ HDMI_TX0_SCL_M0	/ PCIE20X1_2_CLKREQN_M1	/ BT1120_D13	/	/ GPIO4_B7_u AJ28 HDMITX0_SCL_M0
		/ SPI3_CS0_M1	/	/ I2C8_SCL_M3	/ HDMI_TX0_SDA_M0	/ PCIE20X1_2_WAKEN_M1	/ BT1120_D14	/	/ GPIO4_C0_u AJ25 HDMITX0_SDA_M0
SPDIF1_TX_M2	/ PWM6_M1	/ SPI3_CS1_M1	/	/ I2C8_SDA_M3	/ HDMI_TX0_CEC_M0	/ PCIE20X1_2_PERSTN_M1	/ BT1120_D15	/	/ GPIO4_C1_d AK24 HDMITX0_CEC_M0

VCCIO6_1V8 — AC25 VCCIO6_1V8 — C1909 100nF X5R 6.3V C0201 — R1900 0R 1% R0603 — 1 — 2 — VCC_1V8_S0

VCCIO6 — AC26 VCCIO6 — C1908 100nF X5R 6.3V C0201 — R1901 0R 1% R0603 — 1 — 2 — VCC_3V3_S0

RK3588-Socket

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

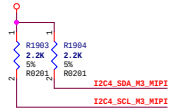
Operating Voltage=1.8V/3.3V

		/SPI4_MISO_M2	/PCIE30X1_1_CLKREQN_M2	/ DP0_HPDIN_M2	/ I2C2_SDA_M4	/ UART6_RX_M1	/ GPIO1_A0_d	A24 MIPI_DCPHY0_RX_PDN_H
SATA1_ACT_LED_M1	/	/SPI4_MOSI_M2	/PCIE30X1_1_WAKEN_M2	/ DP1_HPDIN_M2	/ I2C2_SCL_M4	/ UART6_TX_M1	/ GPIO1_A1_d	A25 MIPI_DCPHY1_RX_PDN_H
	/ PWM0_M2	/SPI4_CLK_M2	/	/ VOP_POST_EMPTY	/ I2C4_SDA_M3	/ UART6_RTSN_M1	/ GPIO1_A2_d	A26 I2C4_SDA_M3_MIPI
	/ PWM1_M2	/SPI4_CS0_M2	/	/ HDMI_TX1_SDA_M2	/ I2C4_SCL_M3	/ UART6_CTSN_M1	/ GPIO1_A3_d	A27 I2C4_SCL_M3_MIPI
	/	/SPI2_MISO_M0	/	/ HDMI_TX1_SCL_M2	/	/	/ GPIO1_A4_d	B25 RTL8111HS_ISOLATEB_L
	/	/SPI2_MOSI_M0		/ HDMI_TX0_HPD_M0	/	/	/ GPIO1_A5_d	B26 HDMITX0_HPDIN_M1
	/	/SPI2_CLK_M0	/	/ HDMI_TX1_HPD_M0	/	/	/ GPIO1_A6_d	C24 HDMITX1_HPDIN_M1
	/ PWM3_IR_M3	/SPI2_CS0_M0	/PCIE30X1_1_PERSTN_M2	/	/ PDM1_SDI0_M1	/	/ GPIO1_A7_u	C25 MIPI_CSI0_PDN1_H
	/	/SPI2_CS1_M0	/PCIE30X4_CLKREQN_M3	/	/ PDM1_SDI1_M1	/	/ GPIO1_B0_u	C27 MIPI_CSI1_PDN1_H
	/	/SPI0_MISO_M2	/PCIE30X4_WAKEN_M3	/	/ PDM1_SDI2_M1	/	/ GPIO1_B1_d	D25 MIPICSI0_PWREN_H
	/	/SPI0_MOSI_M2	/PCIE30X4_PERSTN_M3	/	/ PDM1_SDI3_M1	/ UART4_RX_M2	/ GPIO1_B2_d	D26 MIPICSI1_PWREN_H
SATA0_ACT_LED_M1	/	/SPI0_CLK_M2	/PCIE30X1_0_WAKEN_M2	/	/ PDM1_CLK1_M1	/ UART4_TX_M2	/ GPIO1_B3_d	D27 MIPI_CSI0_PDN0_H
	/	/SPI0_CS0_M2	/PCIE30X1_0_PERSTN_M2	/	/ PDM1_CLK0_M1	/ UART7_RX_M2	/ GPIO1_B4_u	E24 MIPI_CSI1_PDN0_H
	/	/SPI0_CS1_M2	/PCIE30X1_0_CLKREQN_M2	/	/	/ UART7_TX_M2	/ GPIO1_B5_u	E25
	HDMI1_RX_HPDOUT_M2 /	/SPDIF0_TX_M0	/PCIE30X2_WAKEN_M3	/ MIPI_CAMERA1_CLK_M0	/ I2C5_SCL_M3	/ UART1_TX_M1	/ GPIO1_B6_u	E26 MIPI_CAM1_CLKOUT
SATA2_ACT_LED_M1	/ HDMI1_RX_CEC_M2	/ PWM13_M2	/SPDIF1_TX_M0	/PCIE30X2_PERSTN_M3	/ MIPI_CAMERA2_CLK_M0	/ I2C5_SDA_M3	/ UART1_RX_M1	/ GPIO1_B7_u	E27 MIPI_CAM2_CLKOUT
	HDMI1_RX_SCL_M2	/ PWM14_M2	/	/	/ MIPI_CAMERA3_CLK_M0	/ I2C8_SCL_M2	/ UART1_RTSN_M1	/ GPIO1_D6_u	F24 MIPI_CAM3_CLKOUT
	HDMI1_RX_SDA_M2	/ PWM15_IR_M3	/	/PCIE30X2_CLKREQN_M3	/ MIPI_CAMERA4_CLK_M0	/ I2C8_SDA_M2	/ UART1_CTSN_M1	/ GPIO1_D7_u	F25 MIPI_CAM4_CLKOUT

VCCIO4_1V8 — H20 VCCIO4_1V8 — C1907 100nF X5R 6.3V C0201 — R1908 0R 1% R0603 — 1 — 2 — VCC_1V8_S0

VCCIO4 — H21 — C1906 100nF X5R 6.3V C0201

RK3588-Socket



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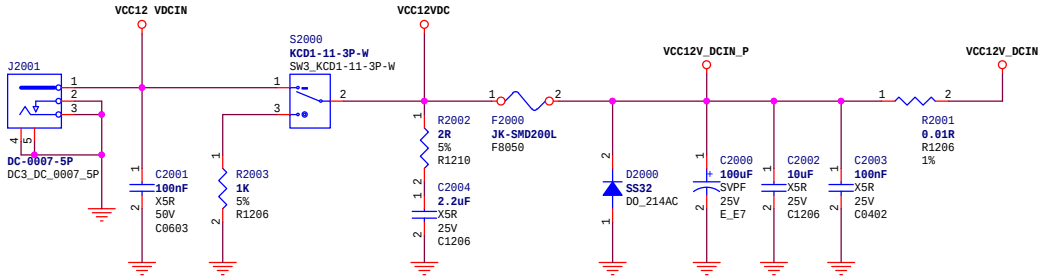
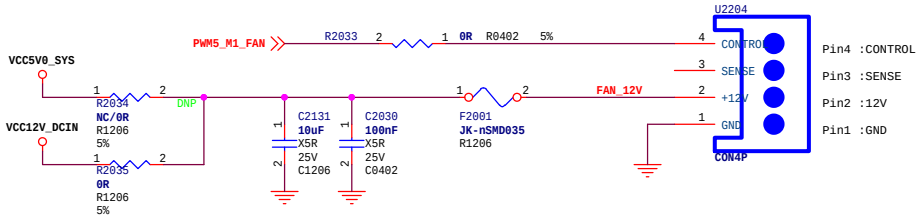
Project:	QuartzPro64 Dev Board Schematic
File:	19.RK3588_1.8V/ 3.3V GPIO
Date:	Tuesday, February 15, 2022
Rev:	V1.0
Designed by:	Rzf
Reviewed by:	
Sheet:	19 of 44

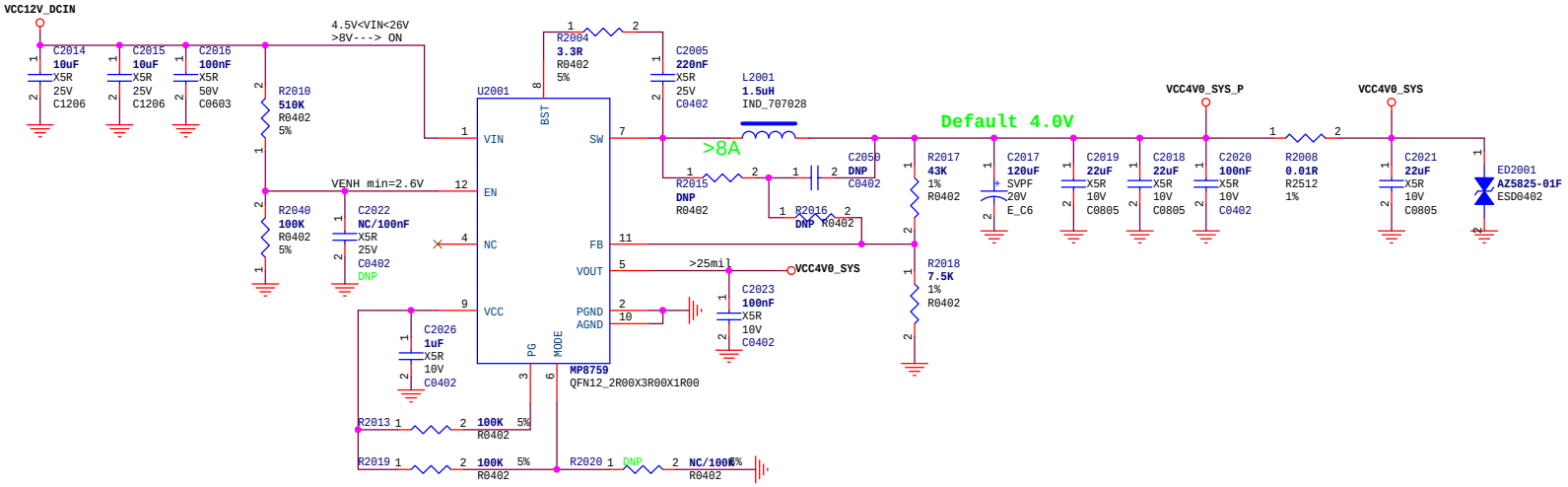
12V/3A DCIN



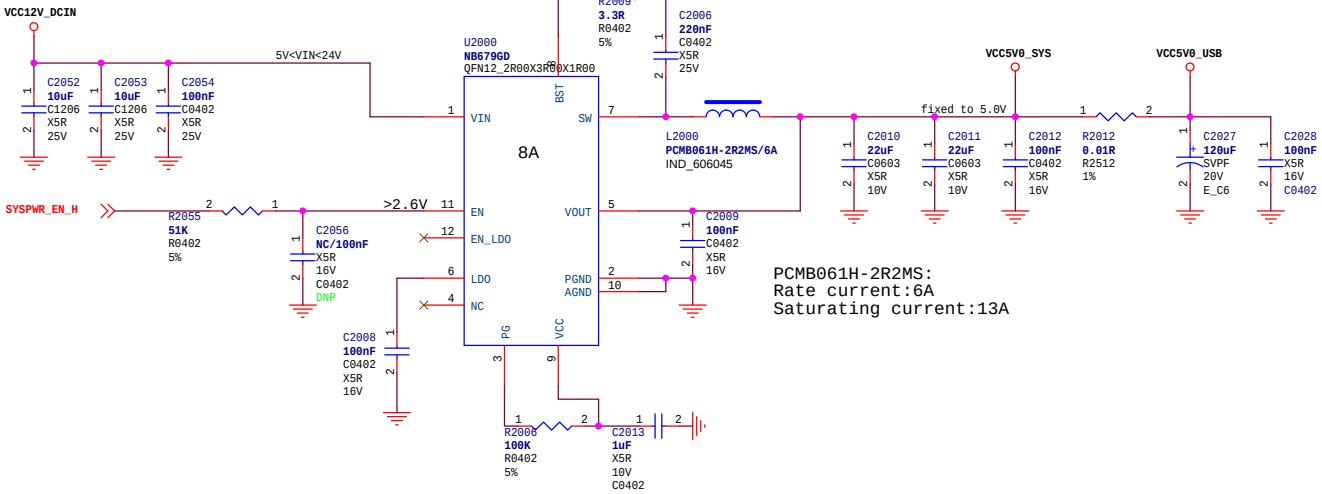
FAN_POWER



VCC4V0_SYS

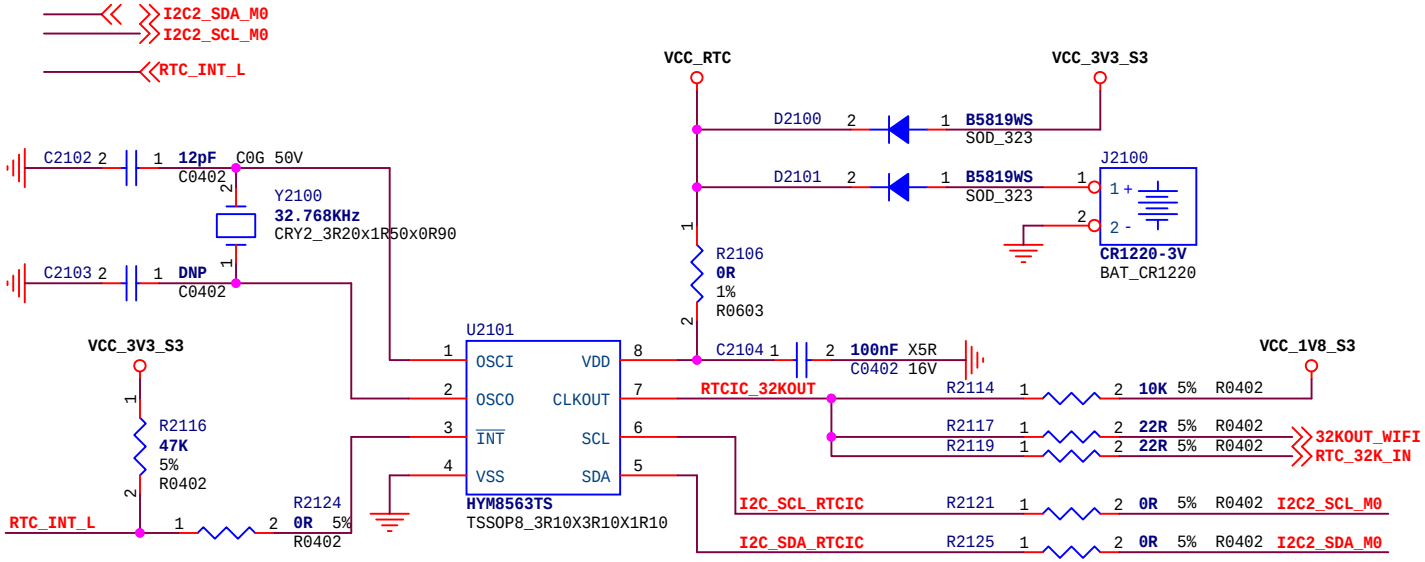


VCC5V0_USB



PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	20.Power_DC IN				
Date:	Saturday, February 19, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Default	Sheet:	20 of 44

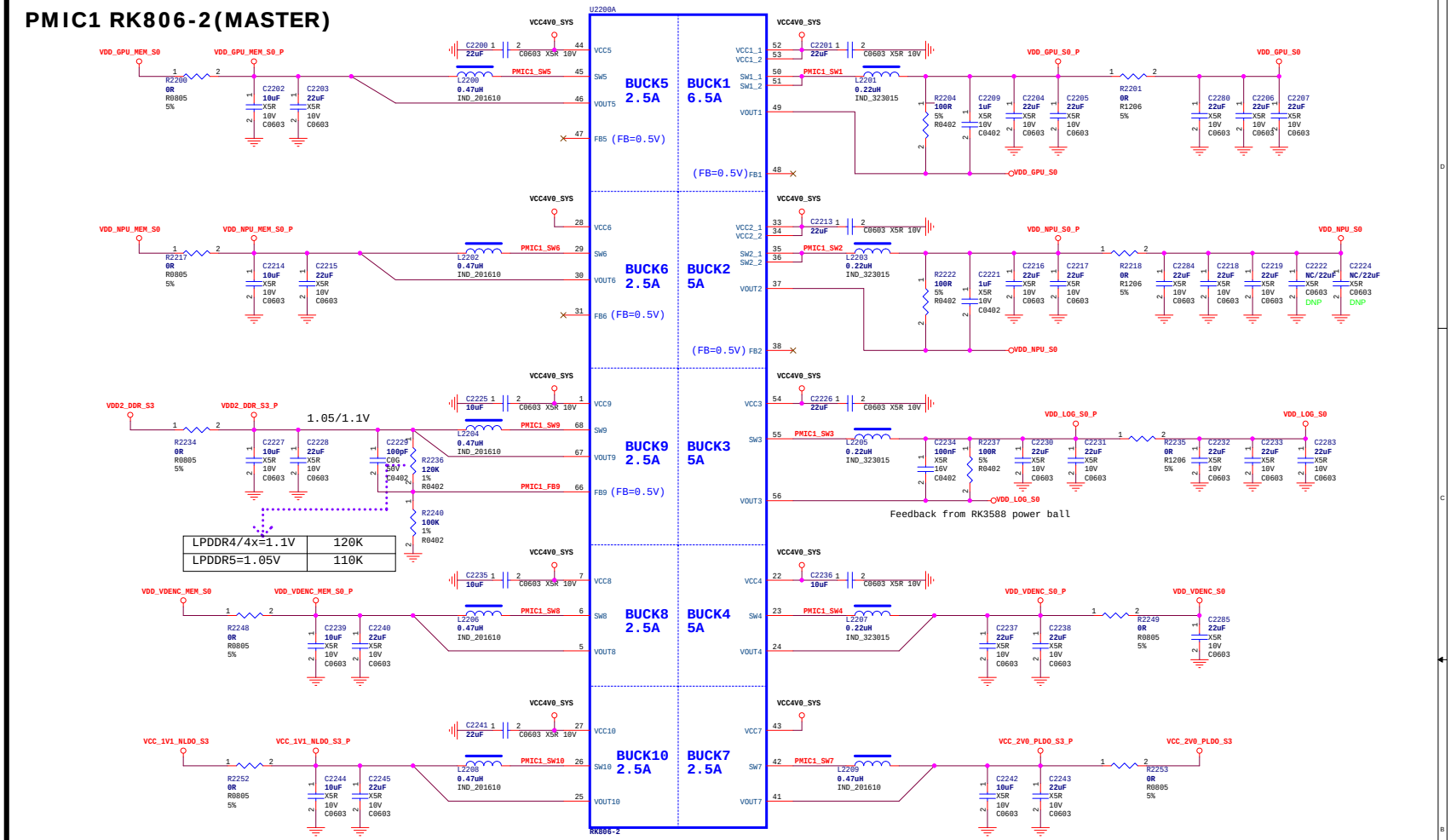
RTC IC

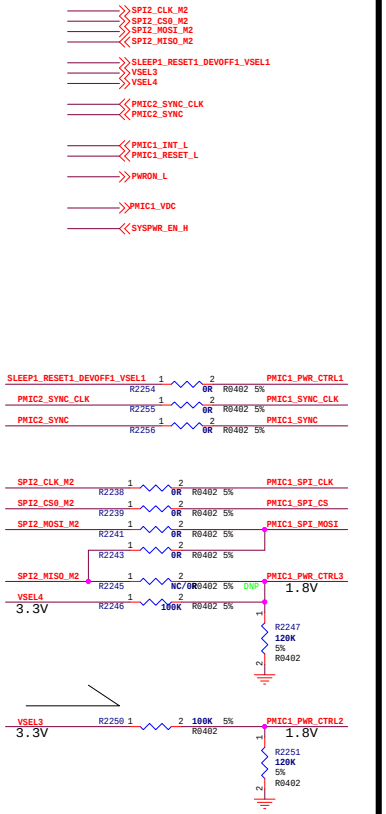


Address:Read A3H,Write A2H

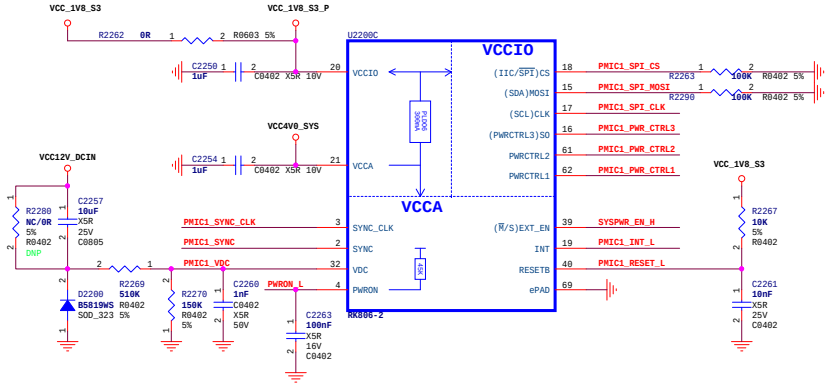
PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**21.Other Power/RTC/PCIE 20 CLK**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Default	Sheet:	21 of 44

PMIC1 RK806-2(MASTER)

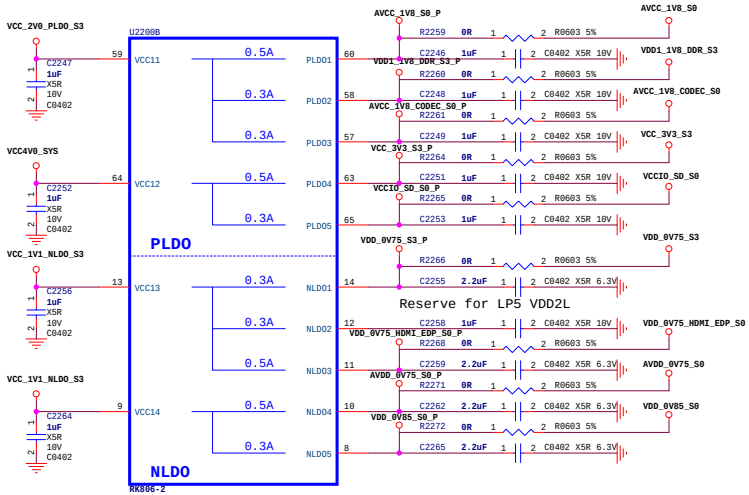




PMIC RK806-2 Managerment

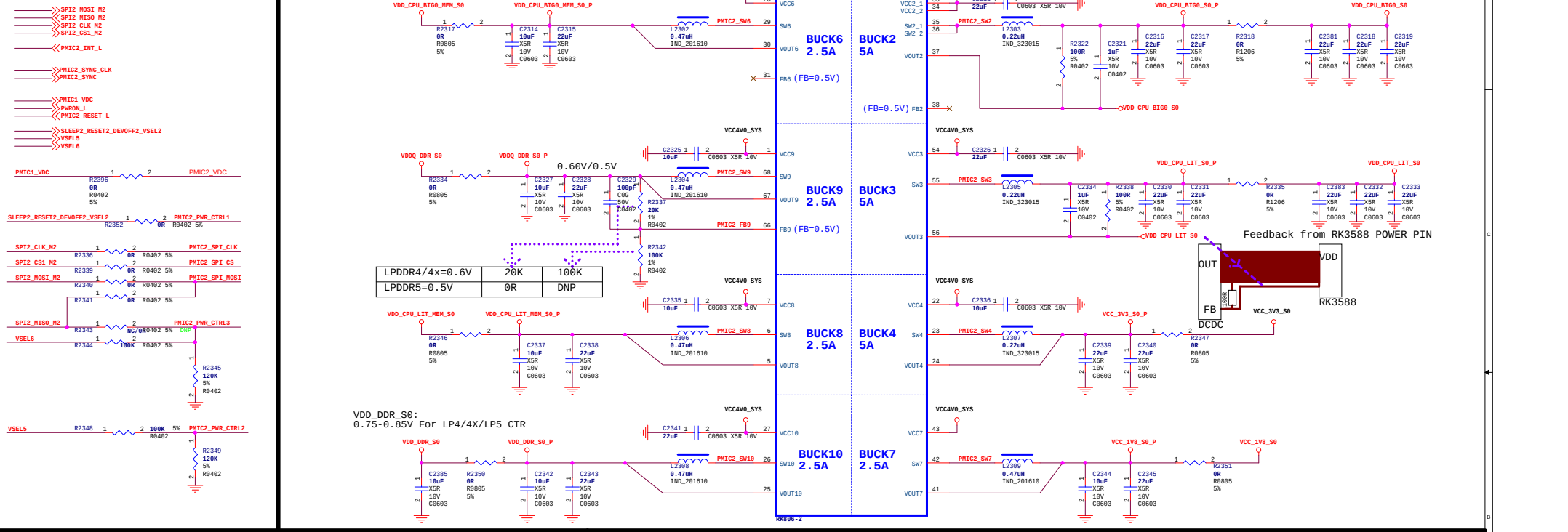


PMIC RK806-2 LDO

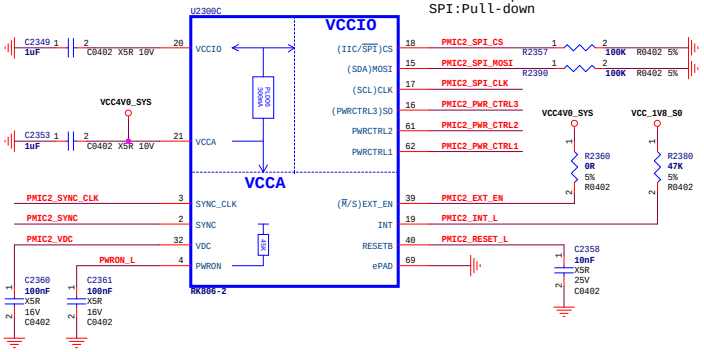


PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	22.Power-PMIC1		
Date:	Tuesday, February 15, 2022	Rev:	V1.3
Designed by:	Rzf	Reviewed by:	Sheet: 22 of 44

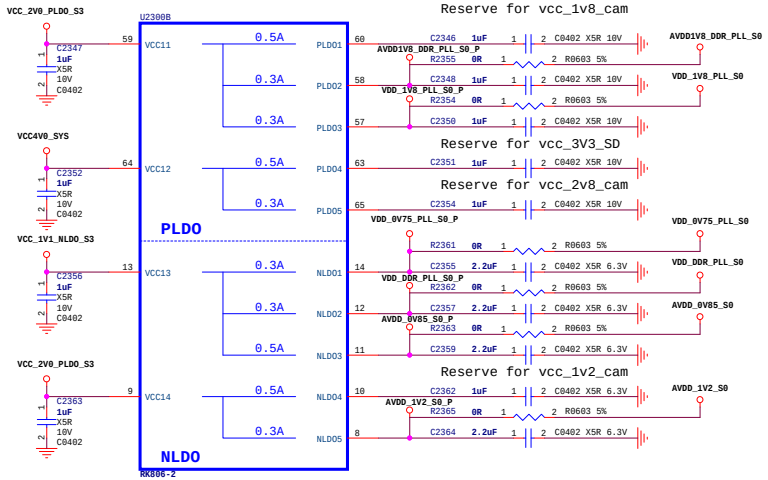
PMIC2 RK806-2(SLAVE)



PMIC RK806-2 Managerment

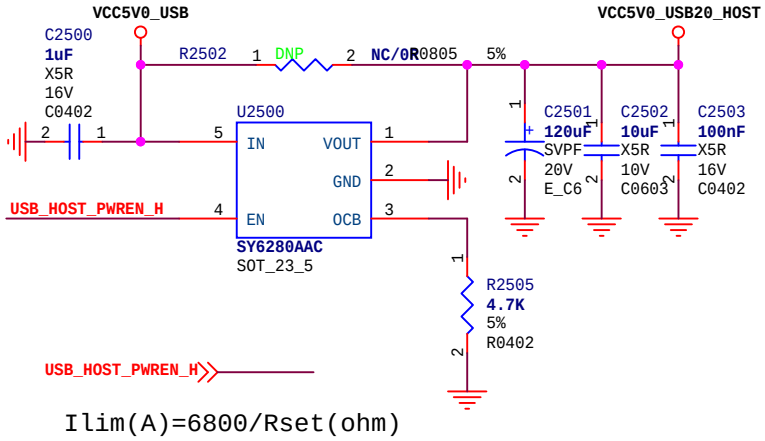


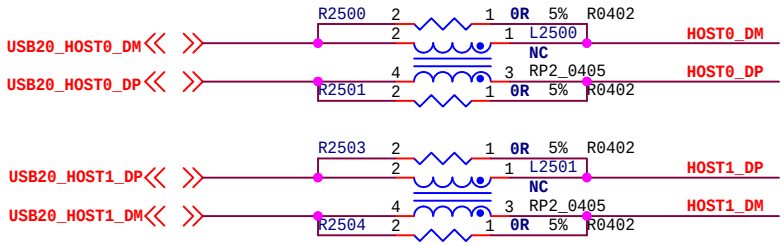
PMIC RK806-2 LDO

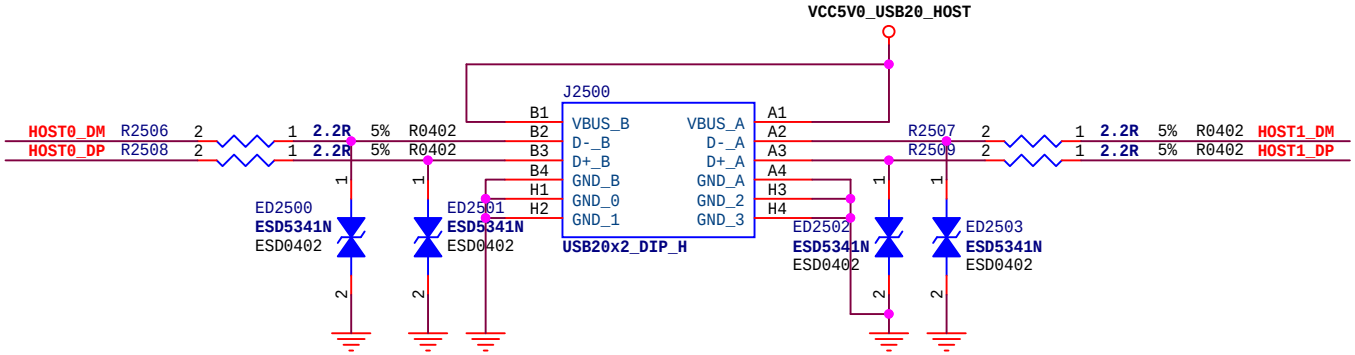


PINE64	PINE64
Project:	QuartzPro64 Dev Board Schematic
File:	23.Power-PMIC2
Date:	Tuesday, February 15, 2022
Rev:	V1.3
Designed by:	Rzf
Reviewed by:	
Sheet:	23 of 44

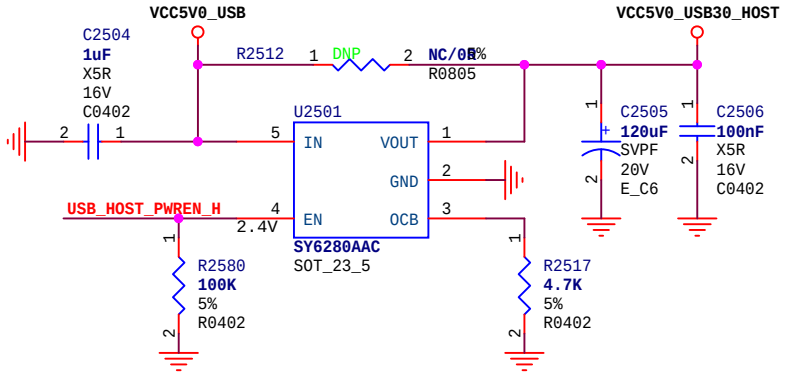
USB2.0 HOST PORT

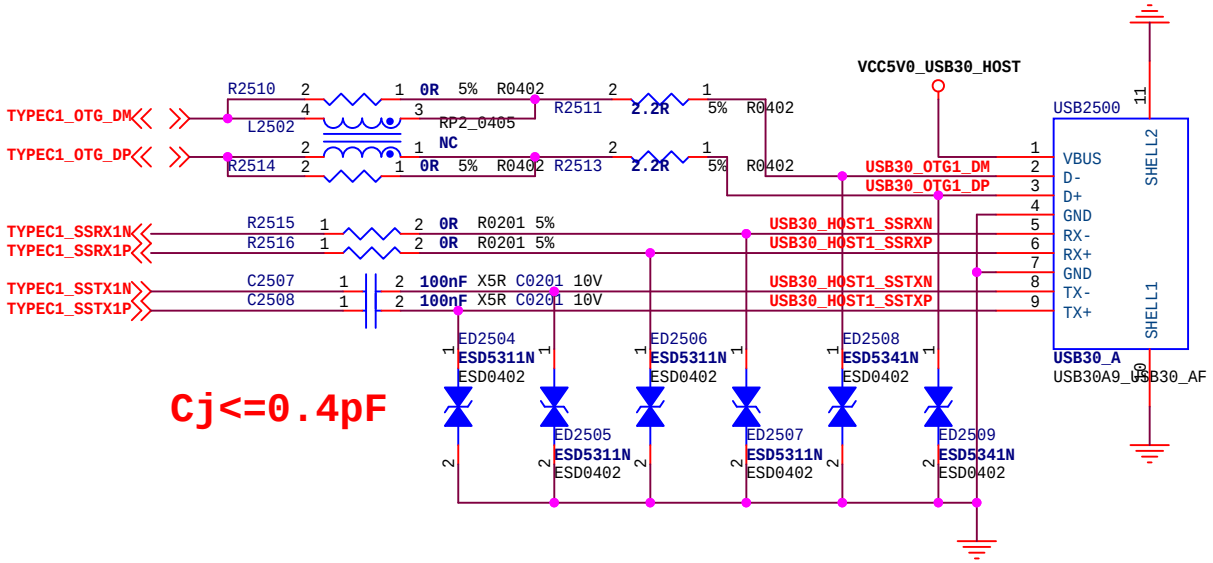






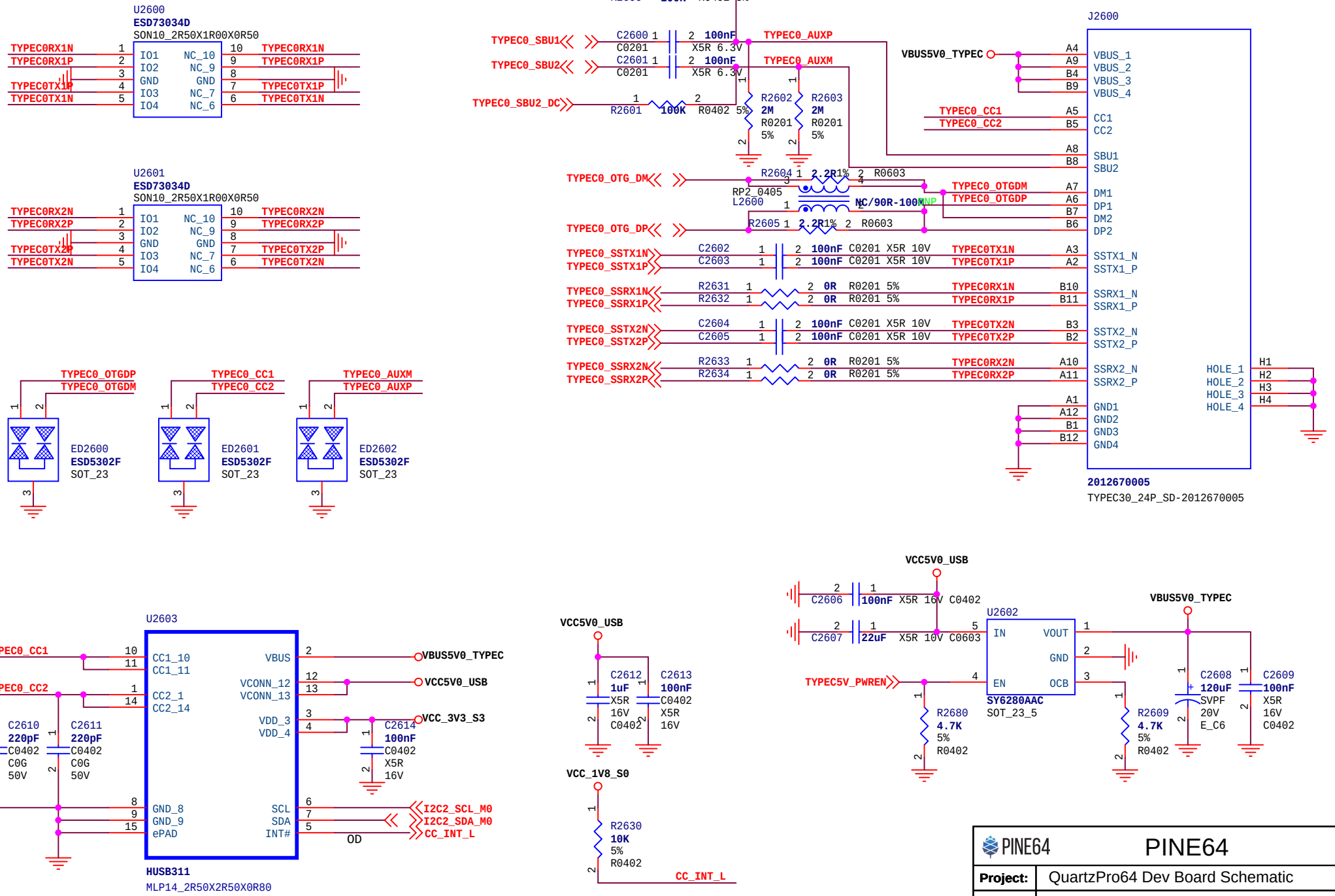
USB3.0 HOST PORT





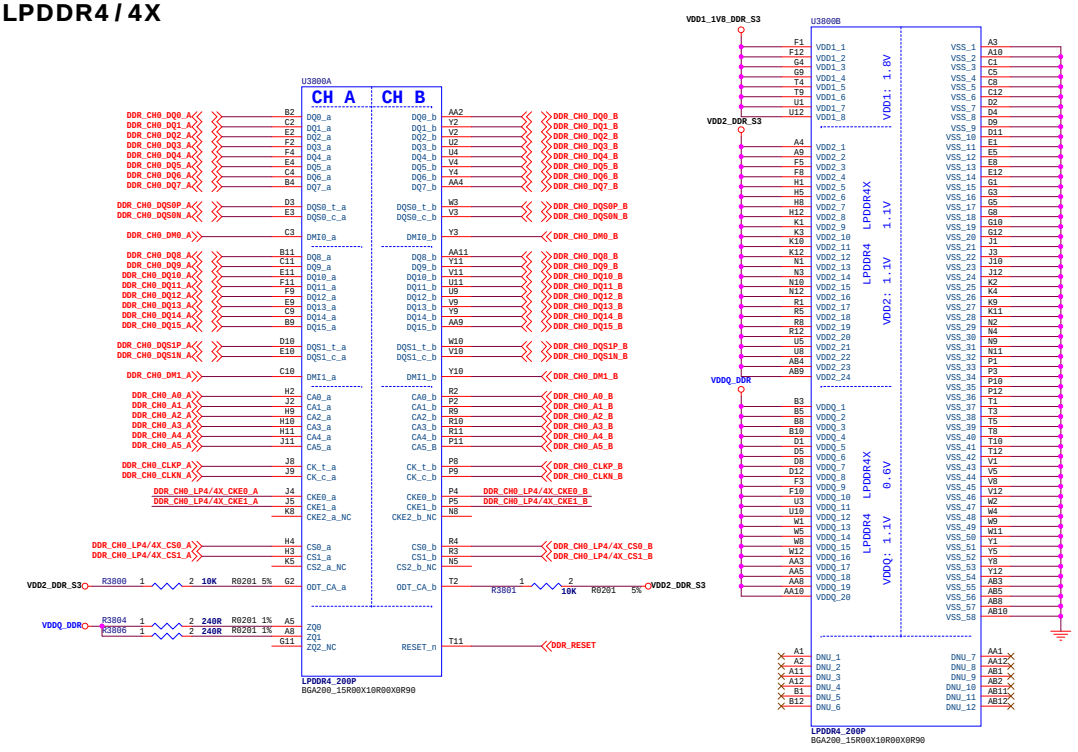
PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**25.USB20/USB30 Port**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	24 of 44

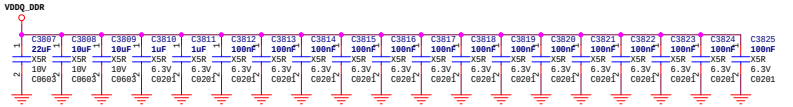
Type-C PORT

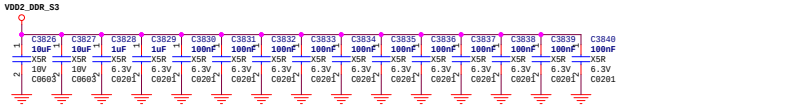


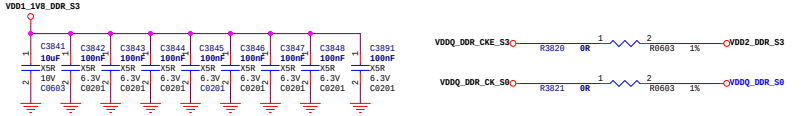
PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	**26.Type-C Port**		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	
Sheet:	25 of 44		

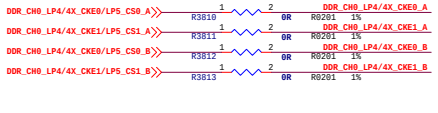
LPDDR4 / 4X

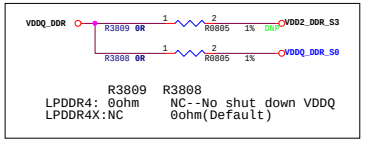






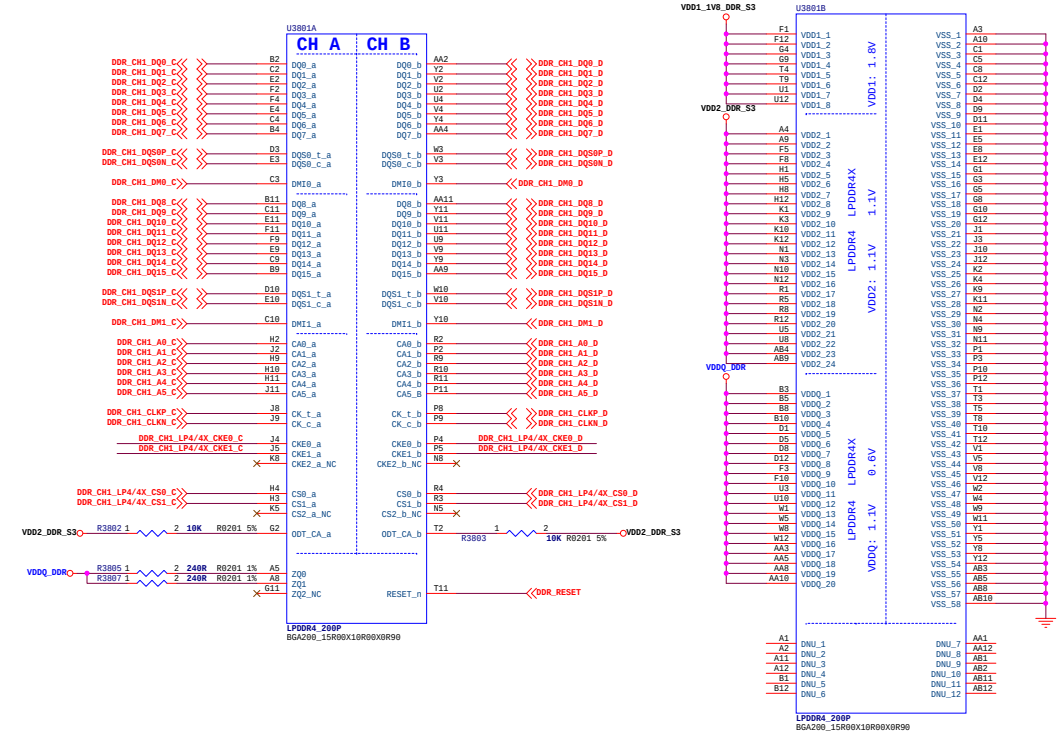


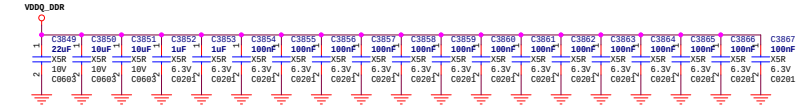


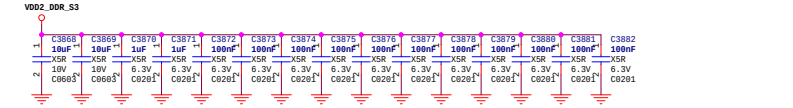


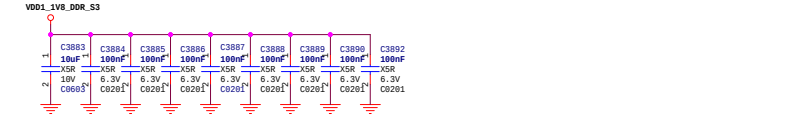
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

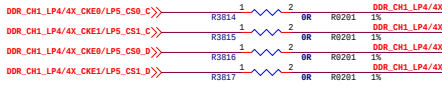
Sequence:VDD1-VDD2-VDDQ





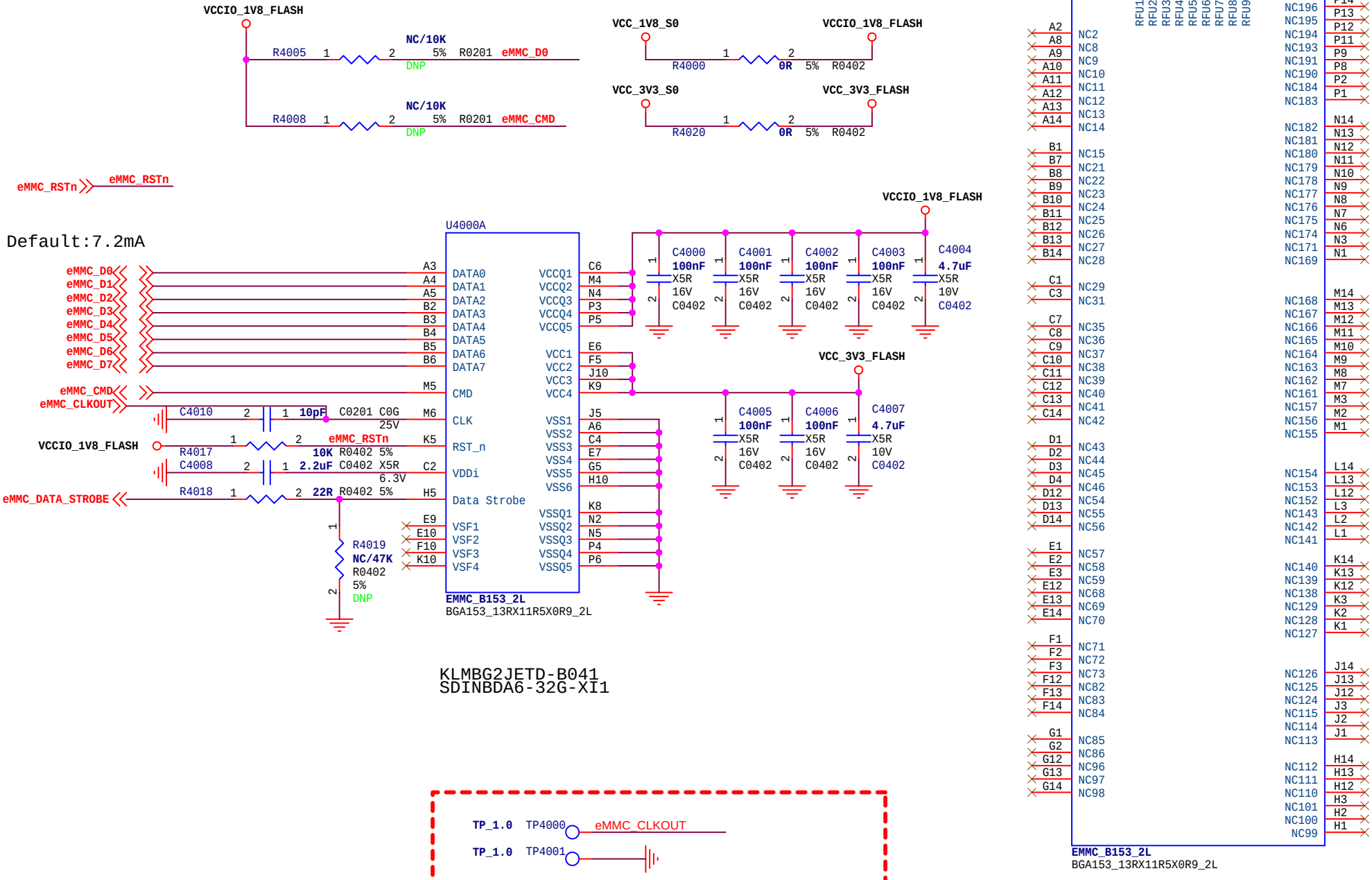




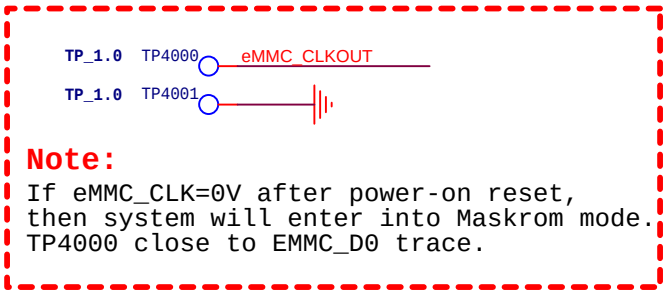


PINE64	PINE64
Project:	QuartzPro64 Dev Board Schematic
File:	38.DRAM-LPDDR4X_200P_1X32bit
Date:	Tuesday, February 15, 2022
Rev:	V1.0
Designed by:	RzT
Reviewed by:	
Sheet	26 of 45

eMMC FLASH

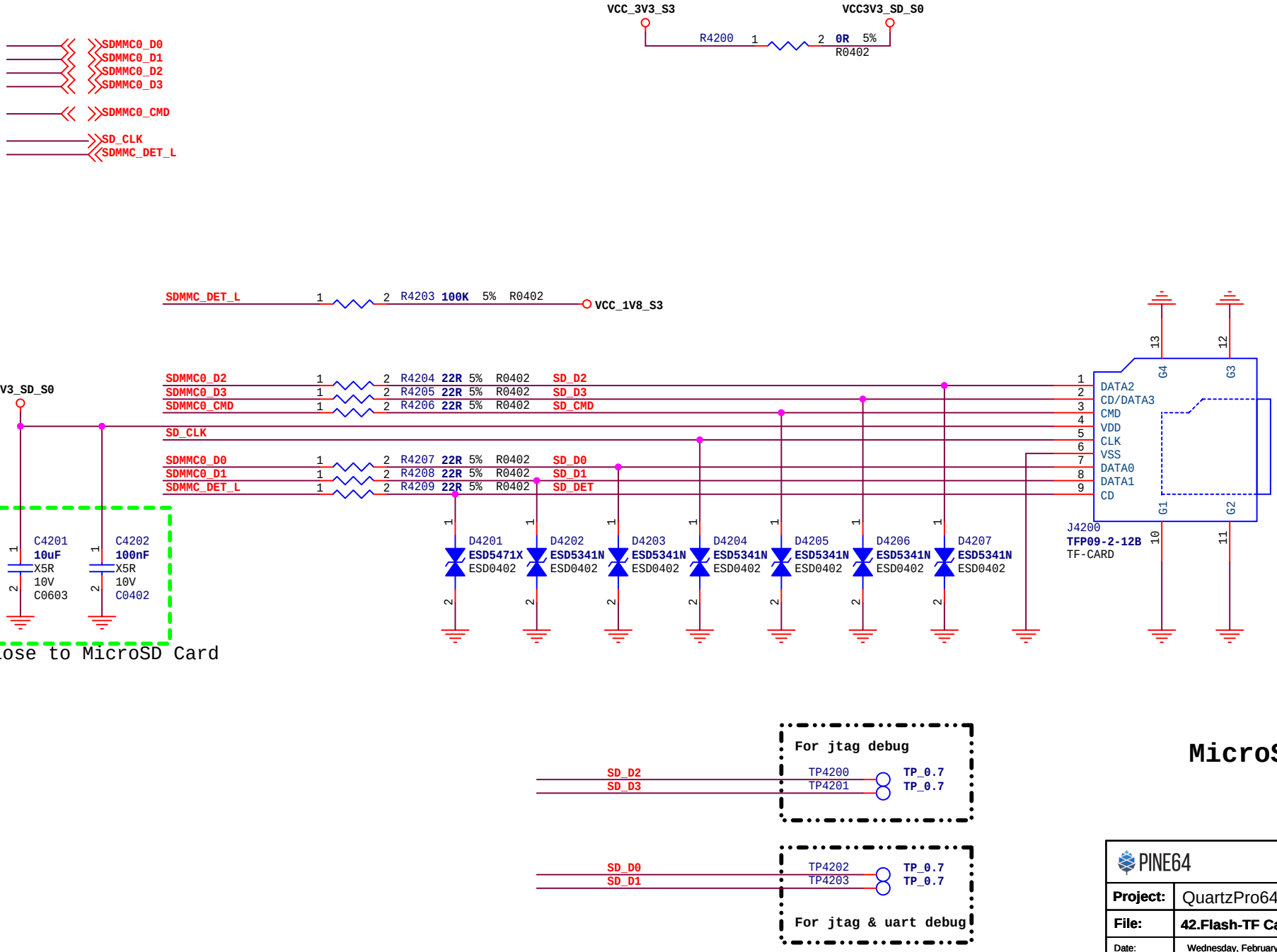


KLMBG2JETD-B041
SDINBDA6-32G-XI1



PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	40.Flash-eMMC Flash		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Sheet: 27 of 44

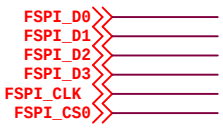
microSD CARD



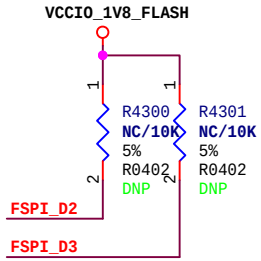
MicroSD Card

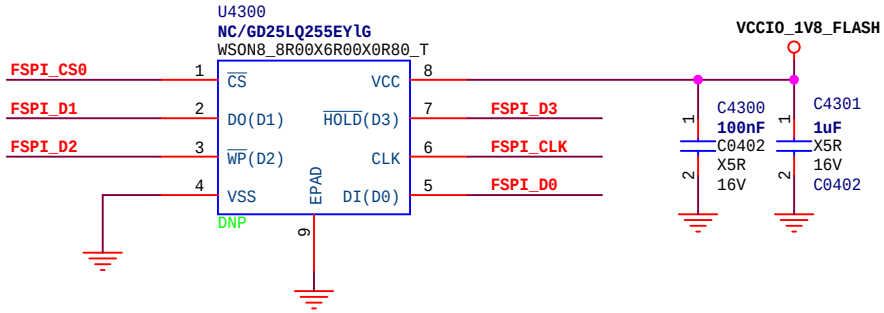
PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**42.Flash-TF Card**				
Date:	Wednesday, February 16, 2022			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	28 of 44

SPI NOR OR NAND Flash (not connected)



Default:5mA





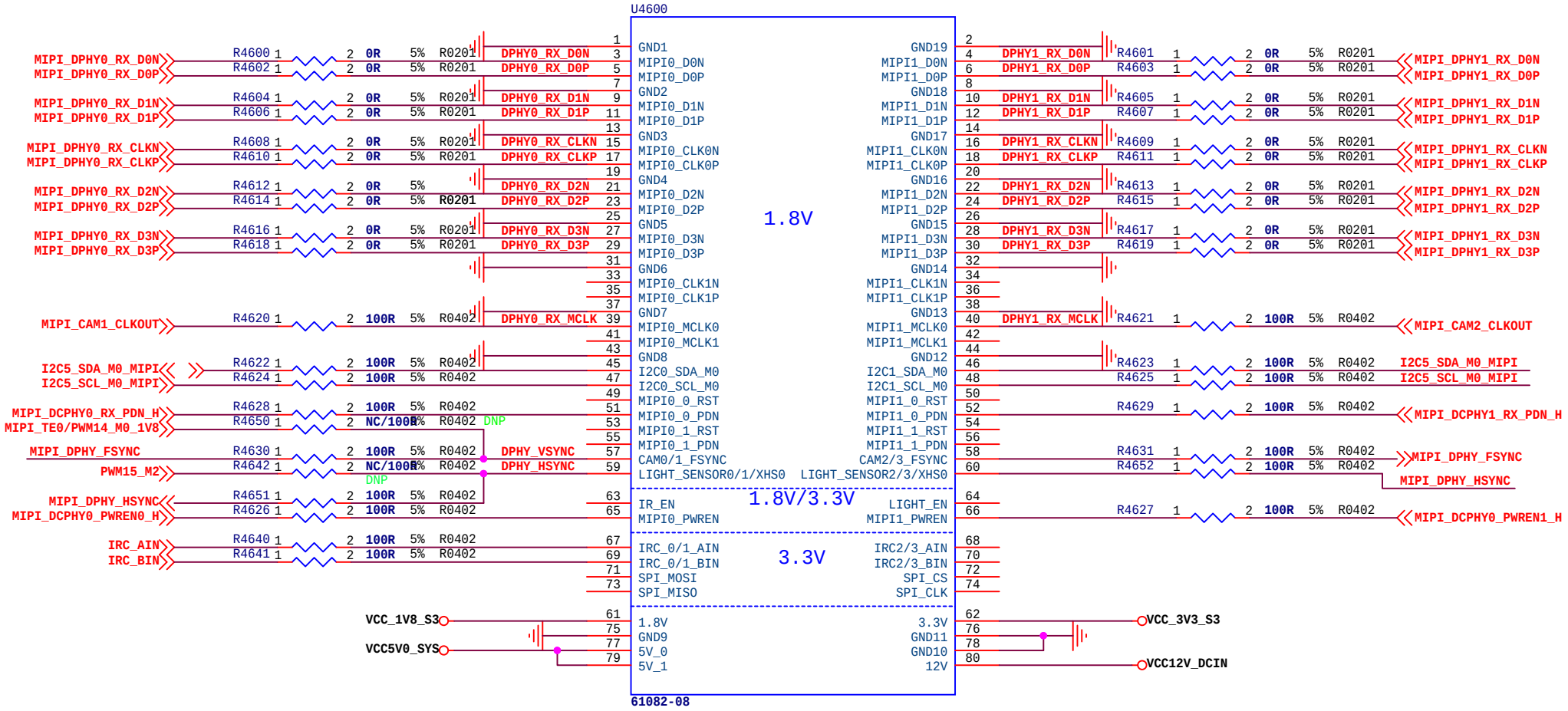
SPI Nor:GD25LQ255EYlG 1.8V

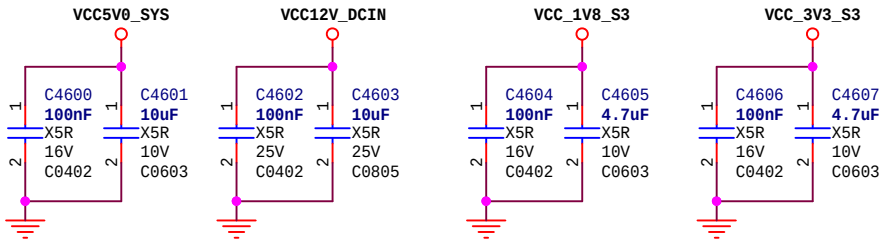
Note:
When using SPI FLASH with only 1 bit, it needs to be stuffed.

PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**43.Flash-SPI FLASH**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Memory Team	Sheet:	29 of 44

MIPI D/C PHY0 DPHY-RX

MIPI D/C PHY1 DPHY-RX

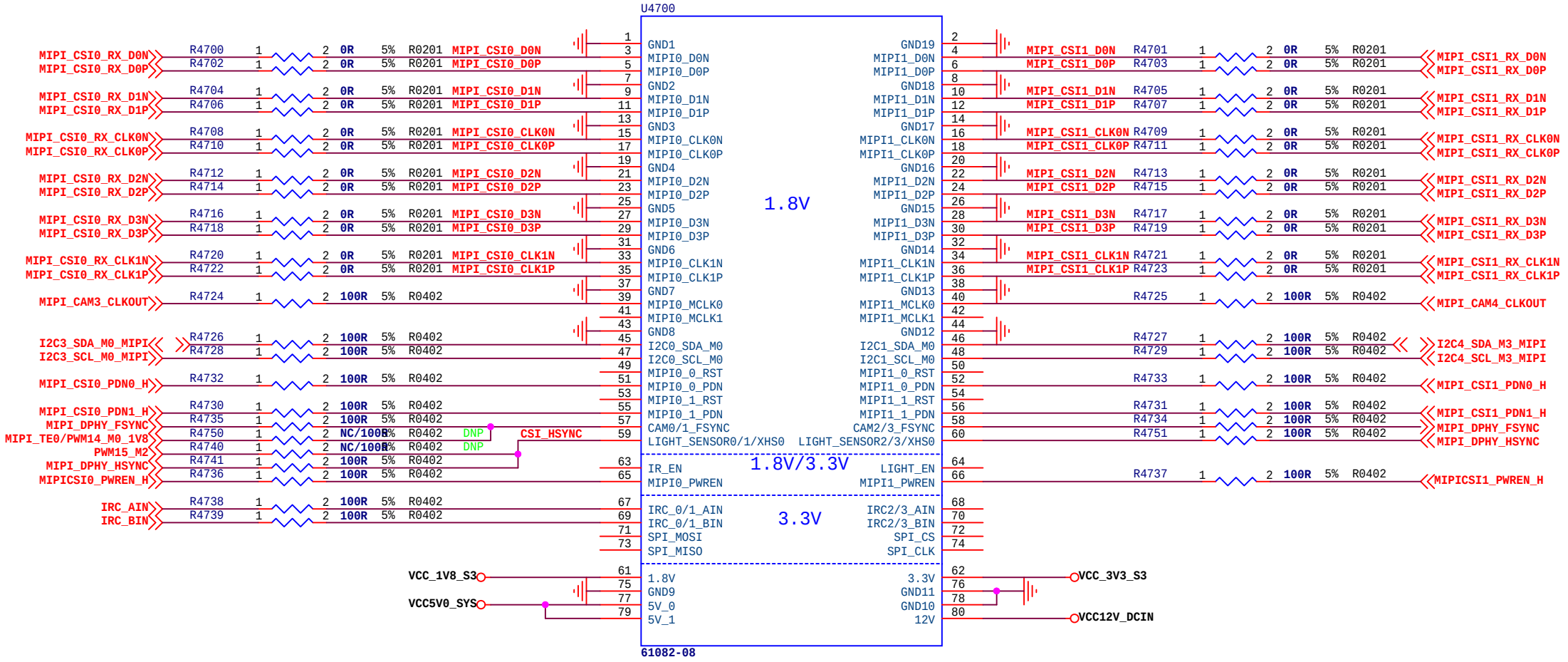




PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**46.VI-Camera D/C PHY_RX**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	30 of 44

MIPI-CSI0_RX

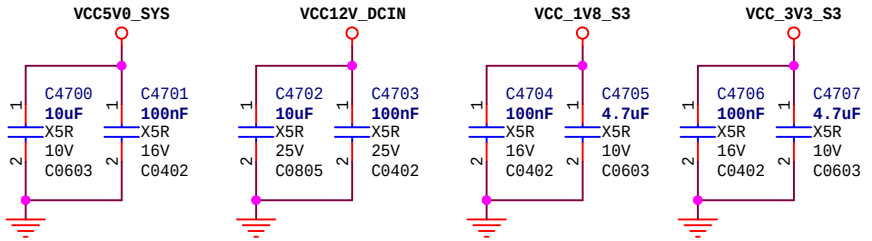
MIPI-CSI1_RX



Note:

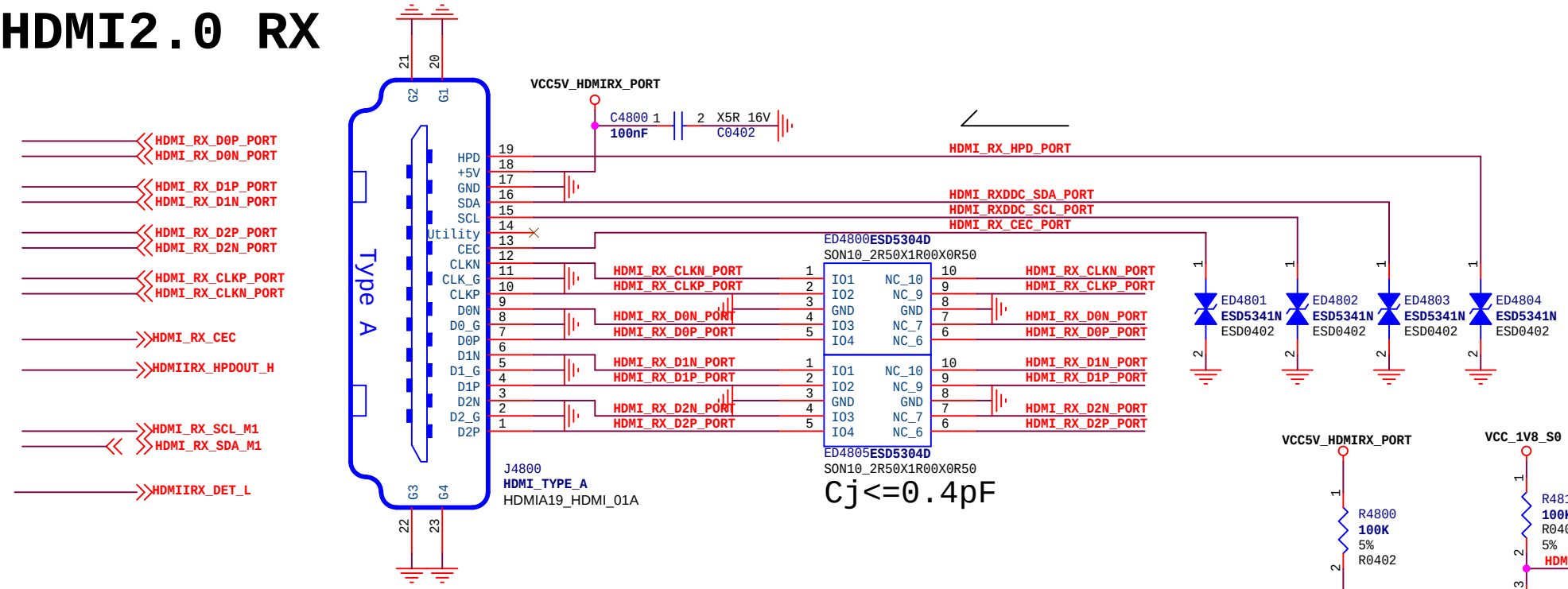
As below pin is for Array-MIC board

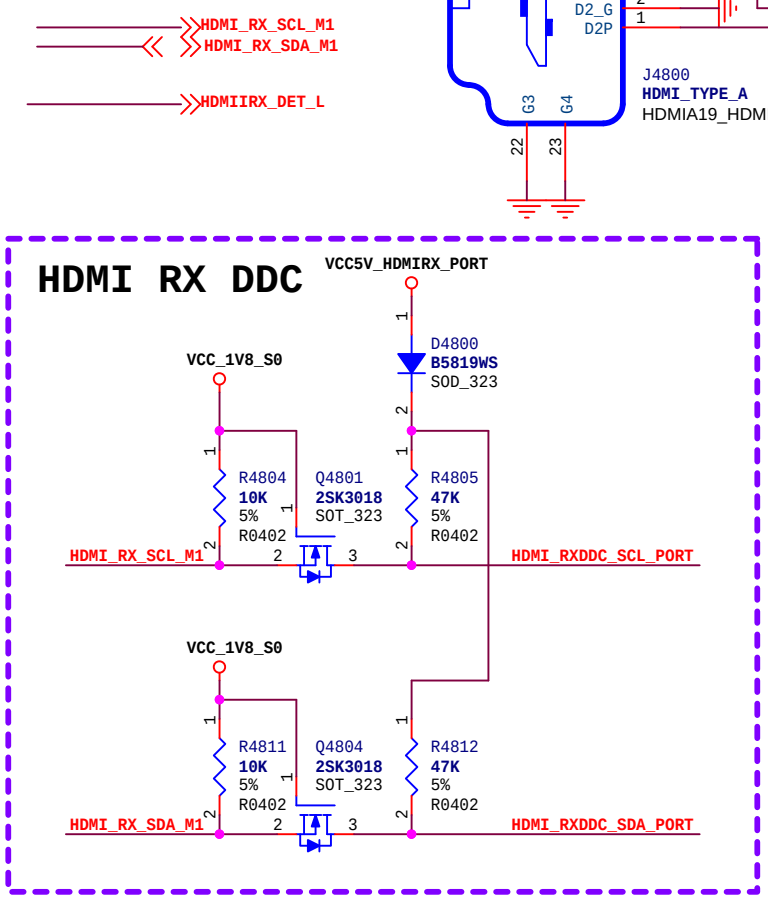
Pin39:I2C_SCL; Pin40:I2C_SDA;
Pin45:PWREN; Pin49:PDM_SDI0;
Pin50:PDM_SDI1; Pin51:PDM_CLK1;
Piin52:PDM_CLK0;Pin65:PDM1_SDI2;
Pin66:PDM1_SDI3

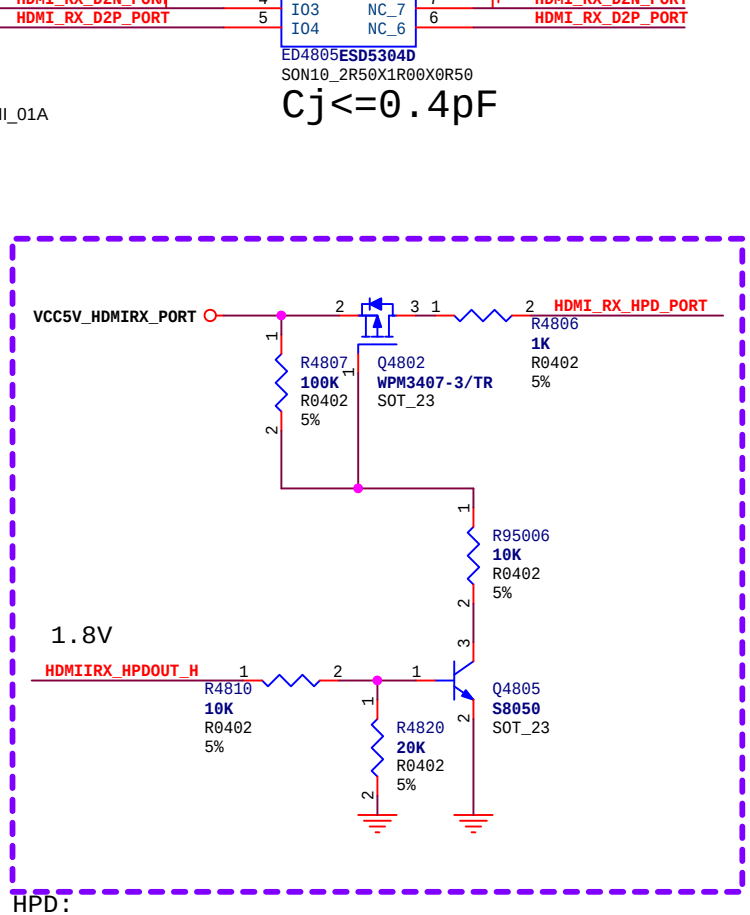


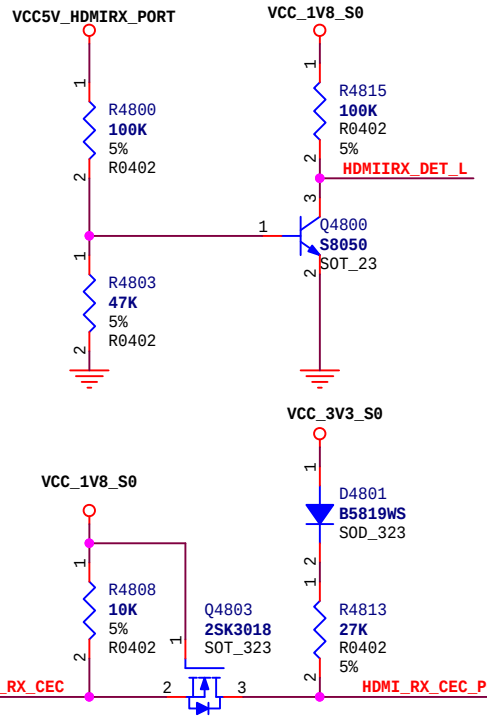
PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	**47.VI-Camera_MIPI-CSI**		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	
Sheet:	31 of 44		

HDMI2.0 RX





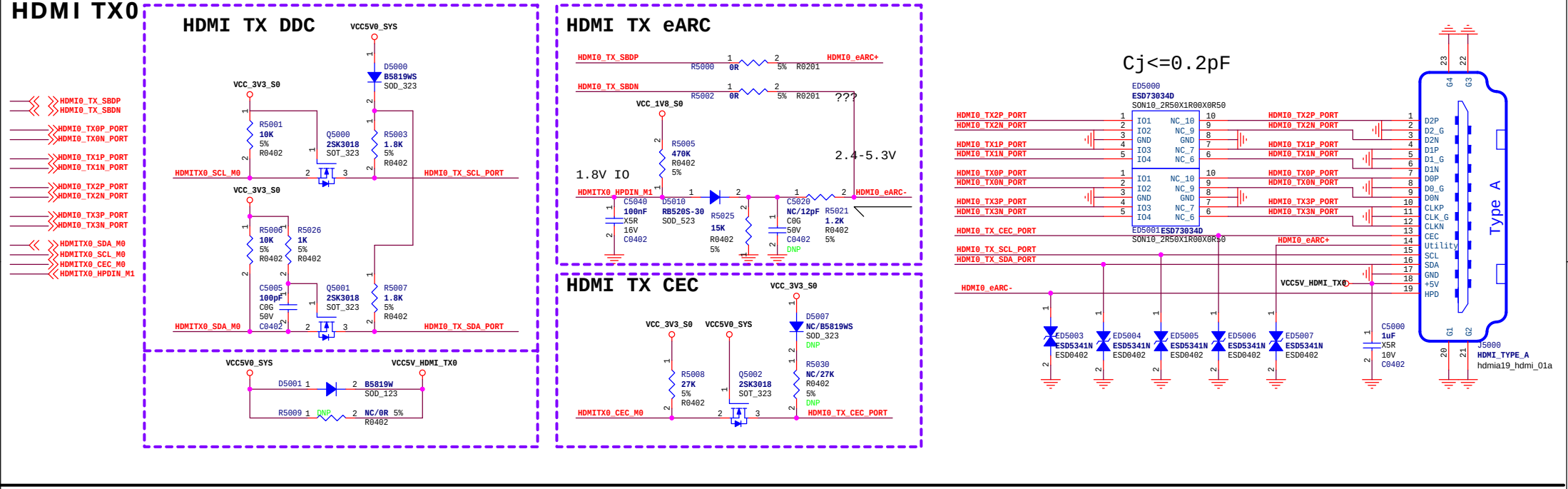




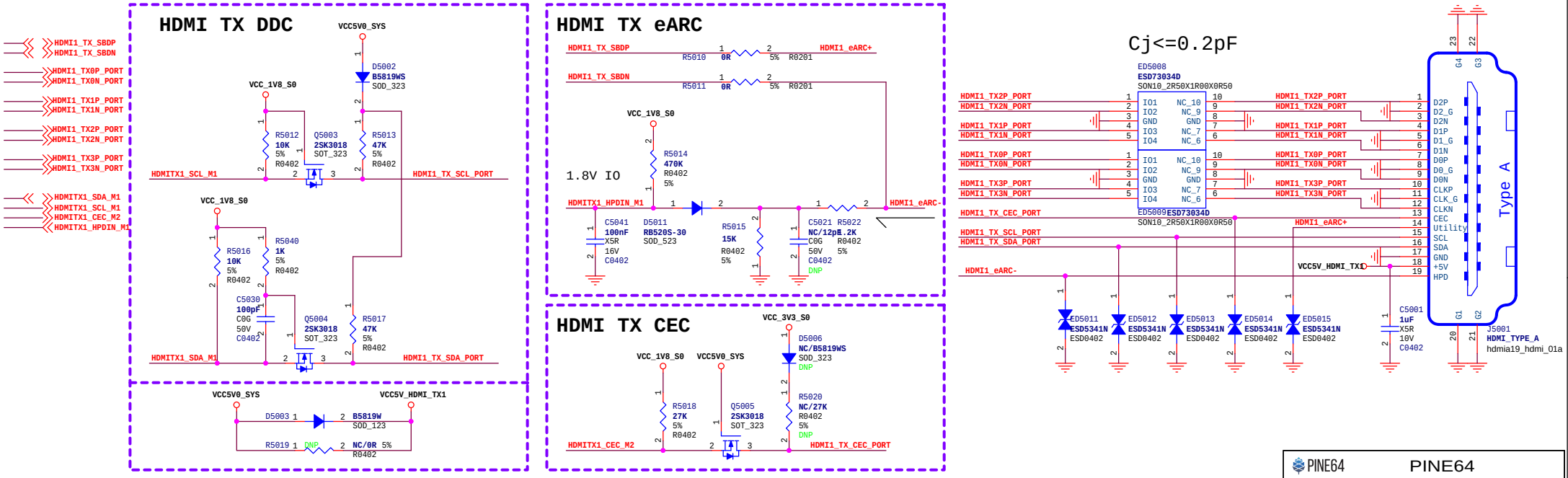
HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V.

PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	**48.VI-HDMI2.0 RX**		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Sheet: 32 of 44

HDMI TX0

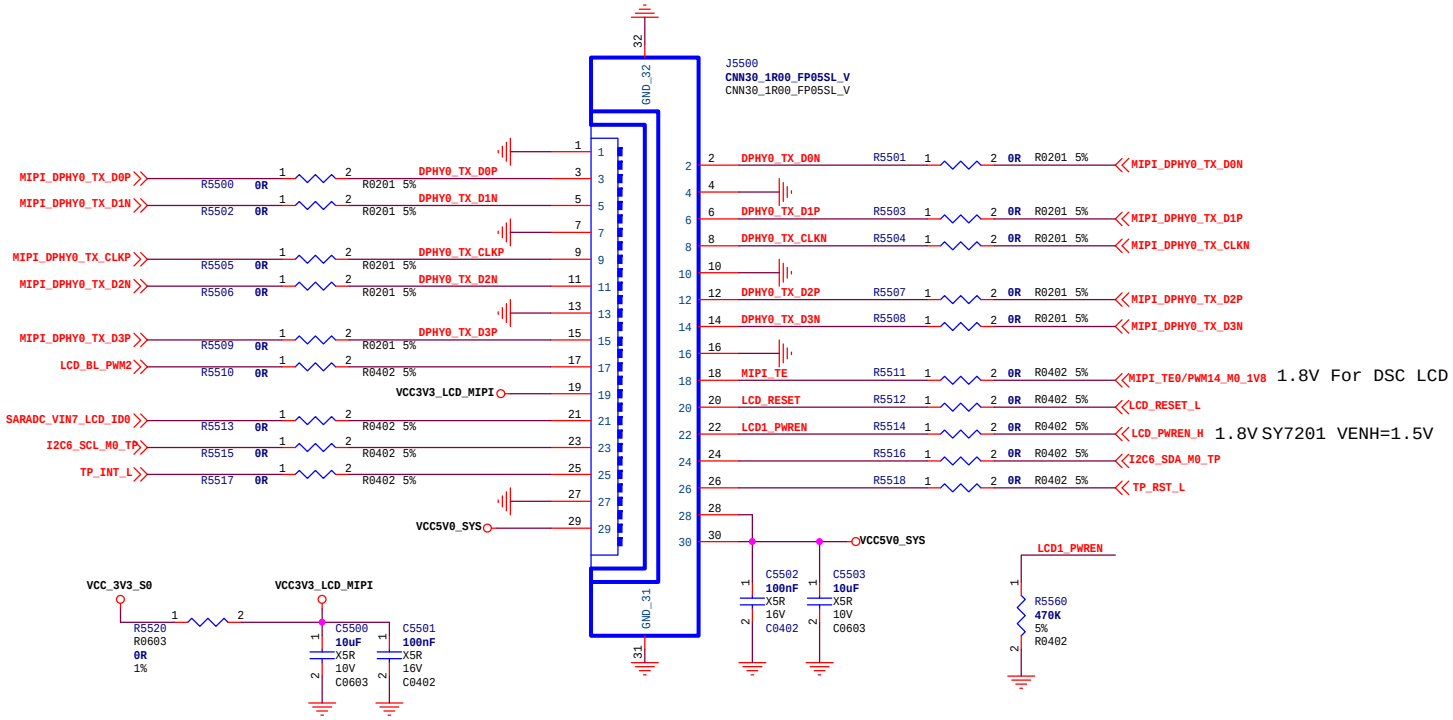


HDMI TX1



PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	50.VO-HDMI2.1 TX				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	33 of 44

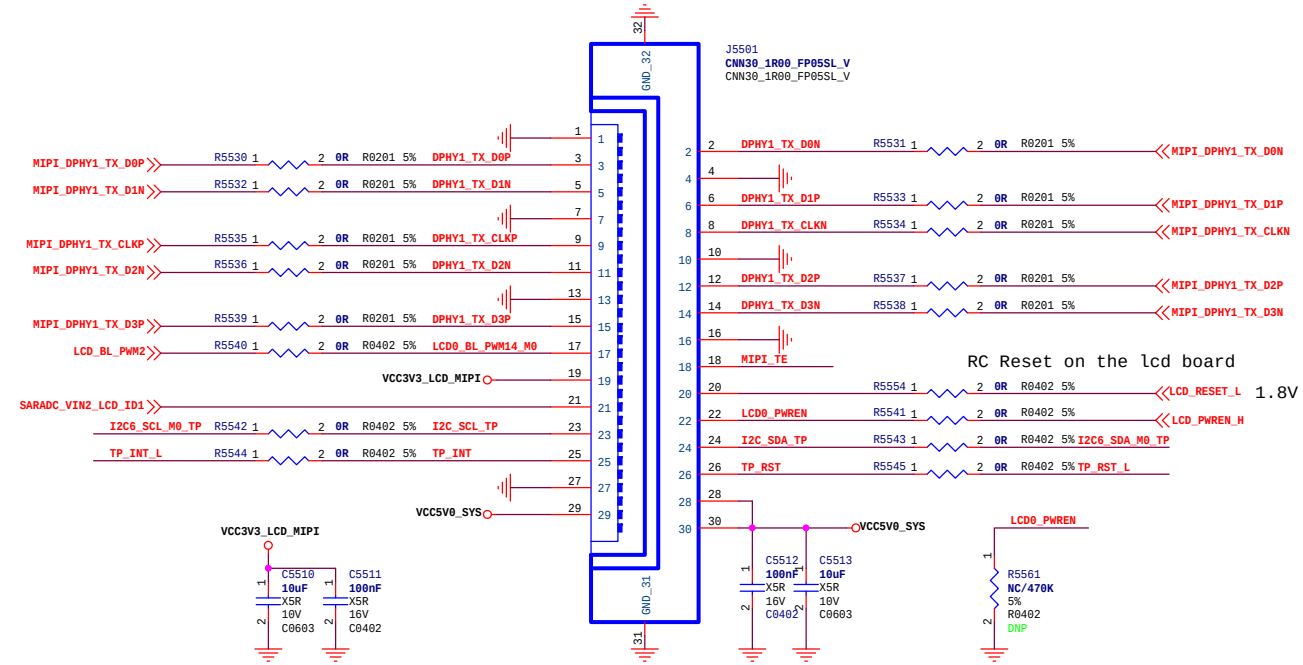
MIPI DPHY0 TX



MIPI FPC Pin List

Pin1 :GND
Pin2 :D0N
Pin3 :D0P
Pin4 :GND
Pin5 :D1N
Pin6 :D1P
Pin7 :GND
Pin8 :CLKN
Pin9 :CLKP
Pin10:GND
Pin11:D2N
Pin12:D2P
Pin13:GND
Pin14:D3N
Pin15:D3P
Pin16:GND
Pin17:LCD_PWM_BL
Pin18:TE
Pin19:VCC_LCD(3.3V)
Pin20:LCD_RST(LCD板RC复位)
Pin21:HW ID
Pin22:LCD_BL_EN(1.8V/3.3V)
Pin23:TP_I2C_SCL(3.3V)
Pin24:TP_I2C_SDA(3.3V)
Pin25:TP_INT(3.3V)
Pin26:TP_RST(3.3V)
Pin27:GND
Pin28:5V0
Pin29:5V0
Pin30:5V0

MIPI DPHY1 TX



PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	55.VO-LCM_MIPI		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Sheet: 34 of 44

PCIe WIFI6/BT Module-2T2R

PCIE20_1_REFCLKP
PCIE20_1_REFCLKN
PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN
PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN
PCIEx1_0_CLKREQn_M1_L
PCIEx1_0_WAKEn_M1_L
PCIEx1_0_PERSTn_M1_L

I2S2_SCLK_TX_M1_BT
I2S2_LRCK_TX_M1_BT
I2S2_SDO_M1_BT
I2S2_SDI_M1_BT
UART8_RX_M1_BT
UART8_TX_M1_BT
UART8_RTSn_M1_BT
UART8_CTSn_M1_BT
BT_REG_ON_H
BT_WAKE_HOST_H
HOST_WAKE_BT_H
WIFI_REG_ON_H
WIFI_WAKE_HOST_H
32KOUT_WIFI

ANT6300
SMA-J-P-H-RA-TH1
ANT5_SMA_RA_TH1
C6300 DNP C0402
C6303 10pF C0G 50V C0402
C6306 DNP C0402

ANT6301
SMA-J-P-H-RA-TH1
ANT5_SMA_RA_TH1
C6301 DNP C0402
C6304 10pF C0G 50V C0402
C6307 DNP C0402

50 Ohm RF trace

ANT6302
ANT_JACK
ANT_JACK
C6302 DNP C0402
C6305 10pFDNP C0G 50V C0402
C6308 DNP C0402

Y6300
XIN_WIFI
XOUT_WIFI
C6309 22pF C0402 C0G 50V
37.4MHz
CRY4_3R20X2R50X0R80
C6310 22pF C0402 C0G 50V

NOTE:
Adjust the load capacitor according to the crystal spec.

U6300
PCIE_PERST_L
XTAL_IN
XTAL_OUT
WL_REG_ON
WL_HOST_WAKE/WL_GPIO_0
NC1
NC2
BT_PCM_OUT
BT_PCM_IN
BT_PCM_SYNC
BT_PCM_CLK
GND10
PCIE_PME_L
CBUCK_0P9
BT_HOST_WAKE
BT_WAKE
NC4
PCIE_TX_P
PCIE_TX_N
PCIE_RX_P
PCIE_RX_N
BT_UART_CTS_N
BT_UART_RTS_N
BT_UART_RXD
BT_UART_TXD
GND14
BT_REG_ON
PCIE_CLKREQ_L
CSR_VLX
GND11
ASR_VLX
ABUCK_1P12
GND12
LPO
GND13
PCIE_RCLK_N
VDDIO
PCIE_RCLK_P
VBAT
GND9
GND8
WL_ANT1
GND7
GND6
GND5
GND4
GND3
GND2
WL_ANT0
GND1

PCIE20_PERSTn_1V8
XIN_WIFI
XOUT_WIFI
WIFI_REG_ON_H
WIFI_WAKE_HOST_H
I2S2_SDI_M1_BT
I2S2_SDO_M1_BT
I2S2_LRCK_TX_M1_BT
I2S2_SCLK_TX_M1_BT
PCIE20_WAKEn_1V8
C6315 4.7uF X5R 10V C0402

BT_HOST_WAKE_H
HOST_WAKE_BT_H
PCIE_TDP C6311 100nF C0201 X5R 6.3V PCIE20_1_RXP/SATA30_1_RXP
PCIE_TDN C6312 100nF C0201 X5R 6.3V PCIE20_1_RXN/SATA30_1_RXN
PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN
UART8_RTSn_M1_BT
UART8_CTSn_M1_BT
UART8_TX_M1_BT
UART8_RX_M1_BT
BT_REG_ON_H
PCIE20_CLKREQn_1V8

This standalone BT-ANT is reserved for AP6275PR3.
Leave PIN48 float for AP6275P, of which BT-ANT is mux with WIFI.

AP6275P/AP6275PR3
MD50_WIFI-AP6275P

VCC3V3_PCIEWL_VBAT
C6316 100nF X5R 16V C0402
C6317 22uF X5R 10V C0603
R6301 0R 1% R0805
VCC_3V3_S0

VBAT:(3.1-3.8V)/1.2A
VDDIO:(1.68-1.98V)/300mA.

L6300 2.2uH IND_303015 1A_DCR<=80mohm
L6301 2.2uH IND_303015 1A_DCR<=80mohm
C6320 4.7uF X5R 10V C0402

VCCIO_WL
C6318 100nF X5R 16V C0402
C6319 4.7uF X5R 10V C0402
R6302 0R R0603 5%
VCC_1V8_S0

REFCLKP_WIFI C6350 100pF C0201 X5R 25V PCIE20_1_REFCLKP
REFCLKN_WIFI C6351 100pF C0201 X5R 25V PCIE20_1_REFCLKN

32KOUT_WIFI
C6323 DNP C0402

32.768KHZ:
+/-25ppm/30-70%/1.8V

WIFI:a/b/g/n/ac/ax 2T2R MIMO
BT:5.0

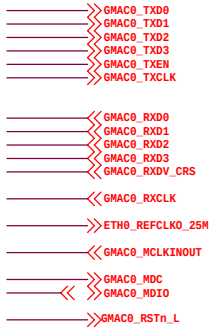
OD
VCCIO_WL
VCC_3V3_S0
R6310 10K 5% R0402
Q6300 2SK3018 SOT_323
R6300 10K 5% R0402
PCIE20_CLKREQn_1V8
PCIEx1_0_CLKREQn_M1_L
R6320 NC/0R R0402 5% DNP

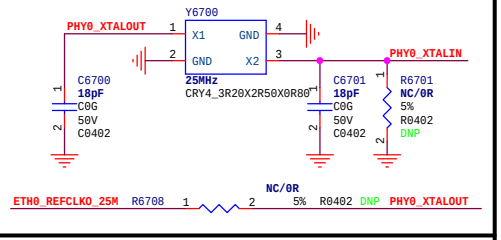
OD
VCCIO_WL
VCC_3V3_S0
R6311 10K 5% R0402
Q6301 2SK3018 SOT_323
R6303 10K 5% R0402
PCIE20_WAKEn_1V8
PCIEx1_0_WAKEn_M1_L
R6321 NC/0R R0402 5% DNP

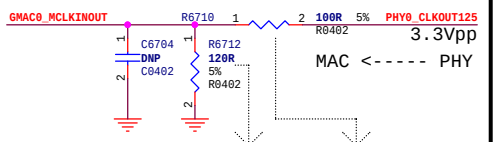
PCIEx1_0_PERSTn_M1_L
R6304 10K 1% R0402
PCIE20_PERSTn_1V8
R6305 12K 5% R0402

PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	63.WIFI/BT-PCIe_2T2R(AP6275PR3)		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Sheet: 35 of 44

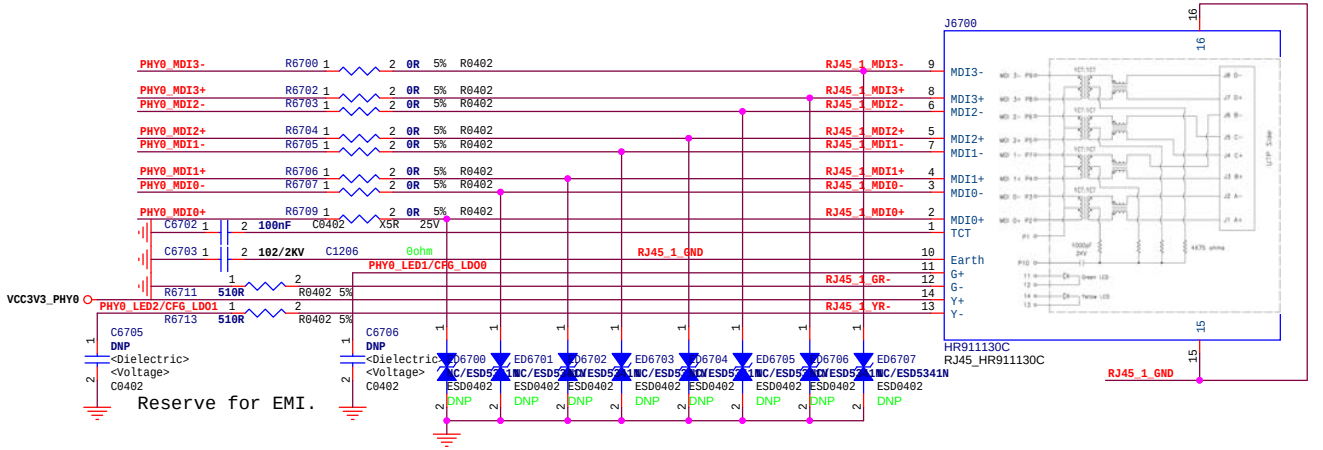
RGMII TO RJ45

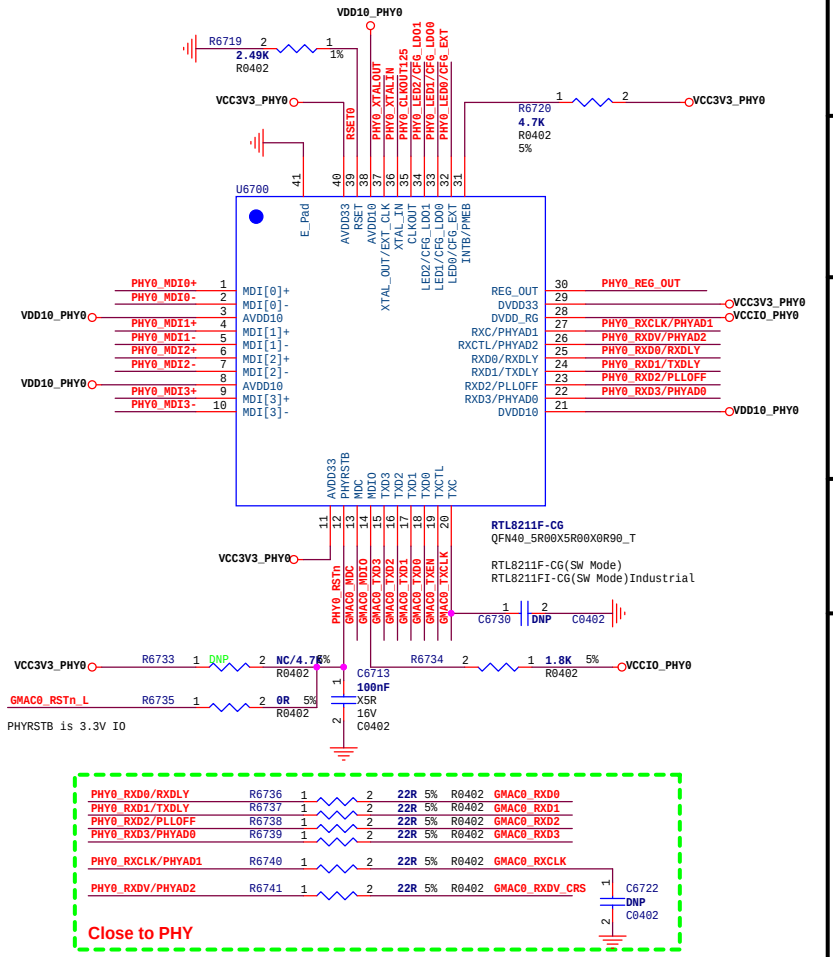


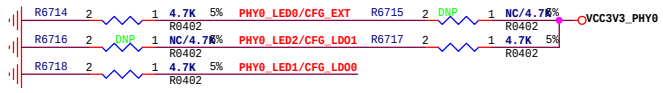




VCCIO_PHY0=3.3V	DNP	22R	
VCCIO_PHY0=1.8V	120R	100R	Default

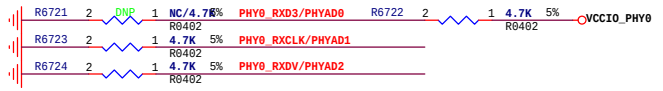






VCC_PHY0_IO Voltage Config

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	



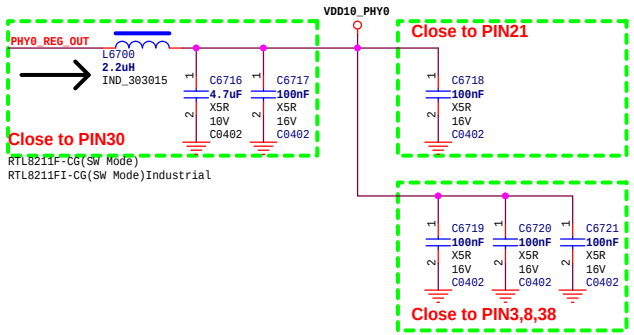
PHY Address Configuration

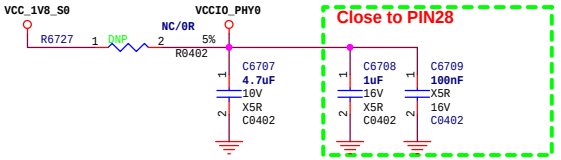
PHY Address	PHYAD[2:0]
1 (default)	3'b001

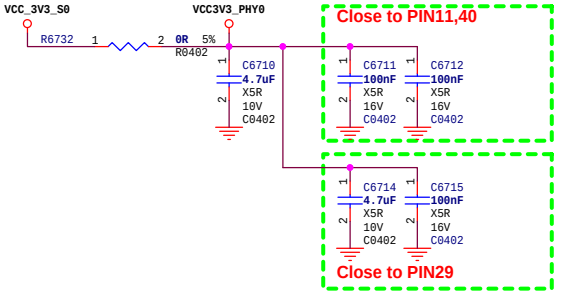
Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDPS mode(Low power mode)



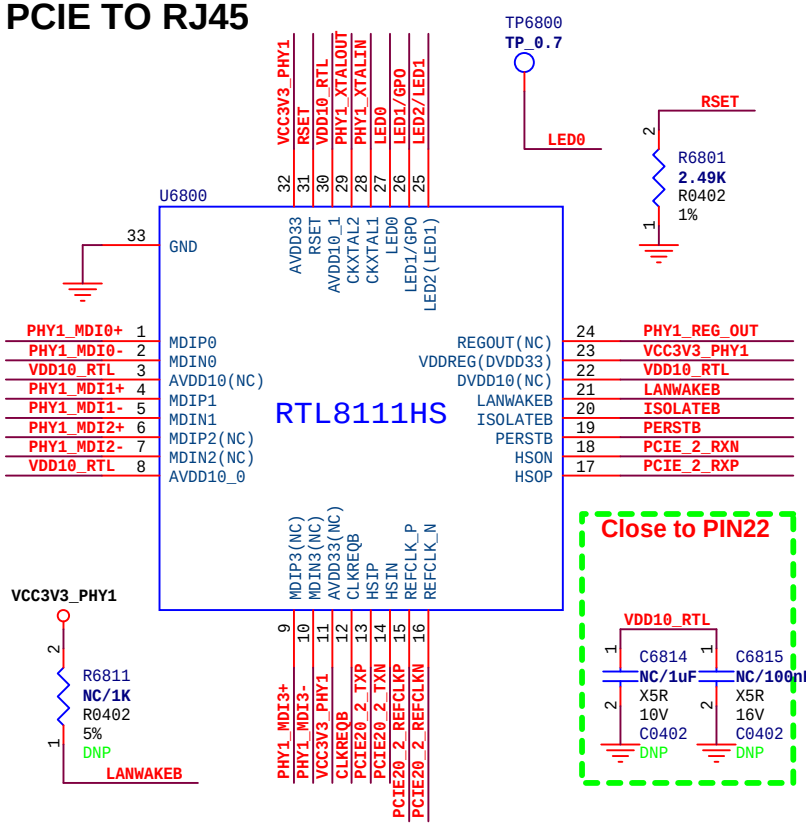


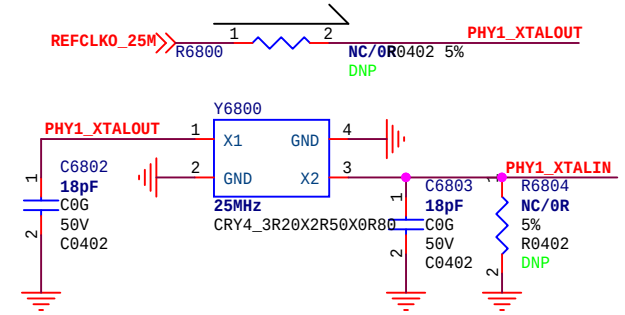


PINE64 PINE64

Project:	QuartzPro64 Dev Board Schematic		
File:	67.Ethernet-GEPHY_RGMII0		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by: Default	Sheet: 36 of 44

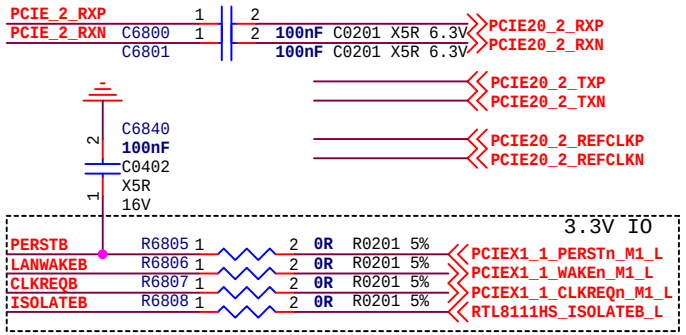
PCIE TO RJ45





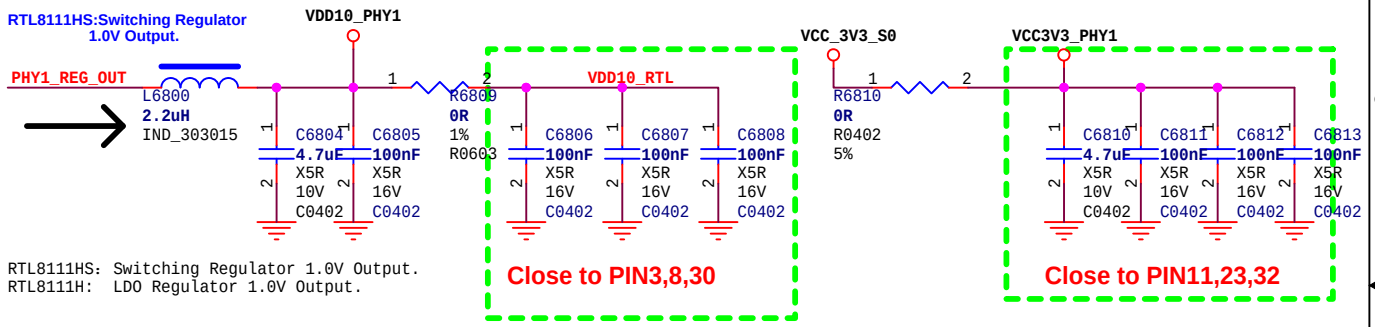
25Mhz Crystal: Stuff Y6800 C6801,No Stuff R6808,R6804
External Clock: Stuff R6804,R6808,No stuff: Y6800,C6801.

CKXTAL1(I): Input of 25Mhz Clock Reference.
CKXTAL2(IO): Input of External Clock Source
Output of 25Mhz Clock Reference.

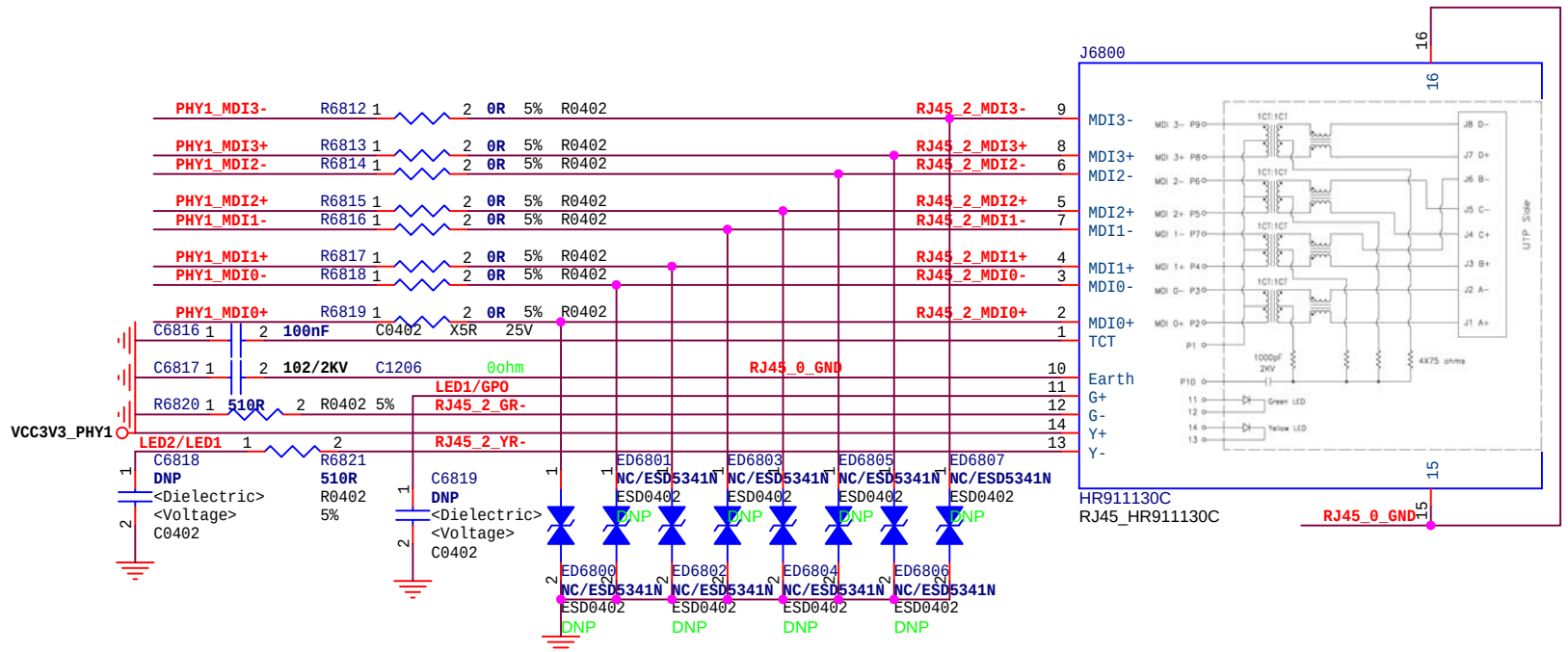


LANWAKEB:Power Management Event (Open Drain;Active Low,1.8V/3.3V compatible input/output mode with a weak external pull resistor)

ISOLATEB :Isolate Pin(Active Low, 1.8V/3,3V compatible input)Used to isolate the RTL8111HS from the PCI Express bus,The RTL8111HS will not drive its PCI Express input as long as the Isolate pin is asserted.

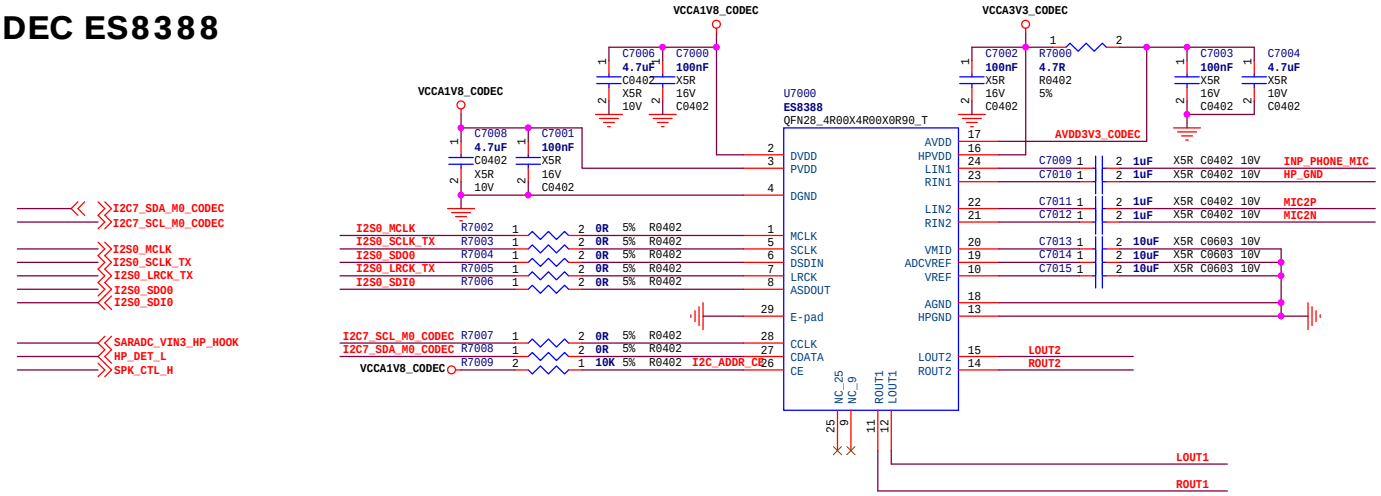


RTL8111HS: Switching Regulator 1.0V Output.
RTL8111H: LDO Regulator 1.0V Output.

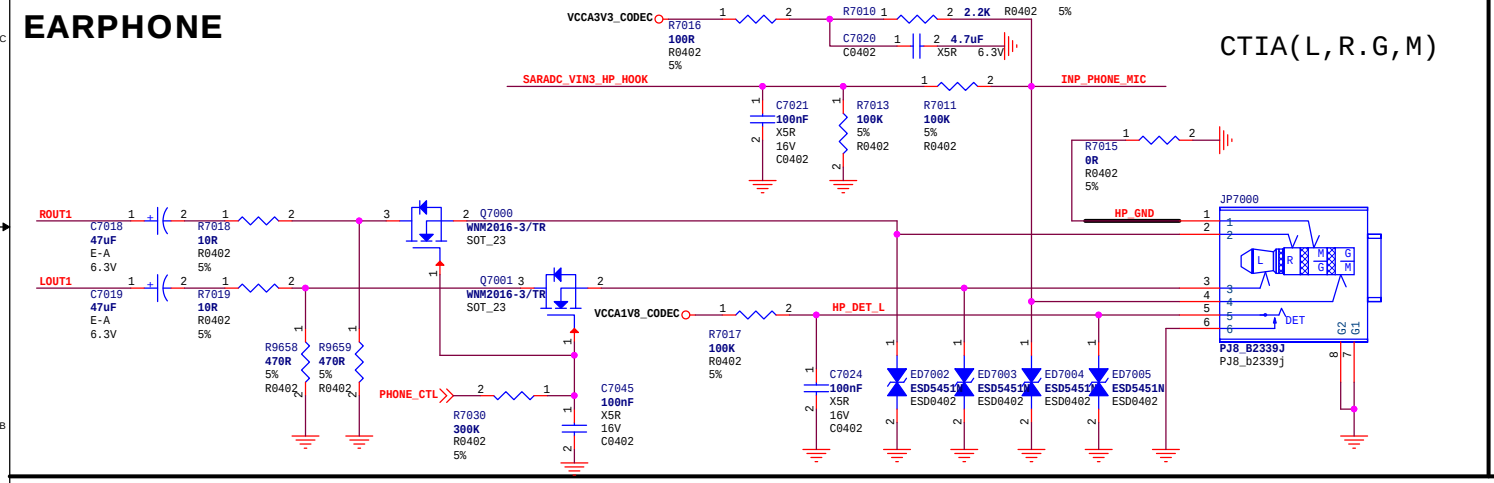


PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	68.PCIE TO RJ45_RTL8111HS				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Default	Sheet:	37 of 44

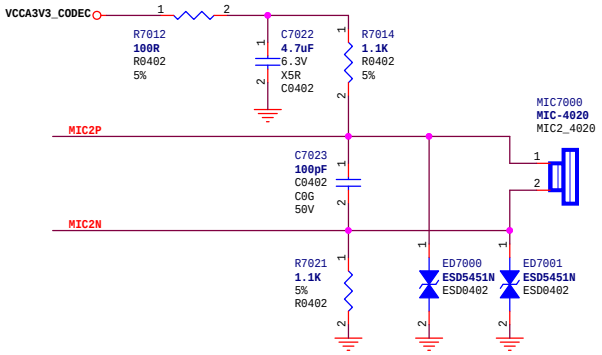
CODEC ES8388



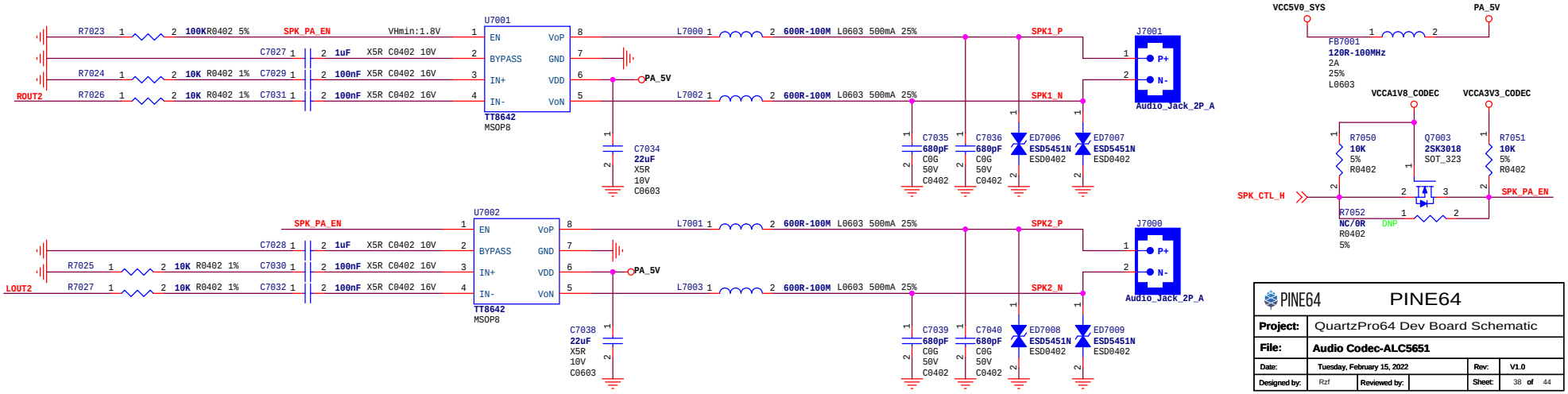
EARPHONE



Analog MIC

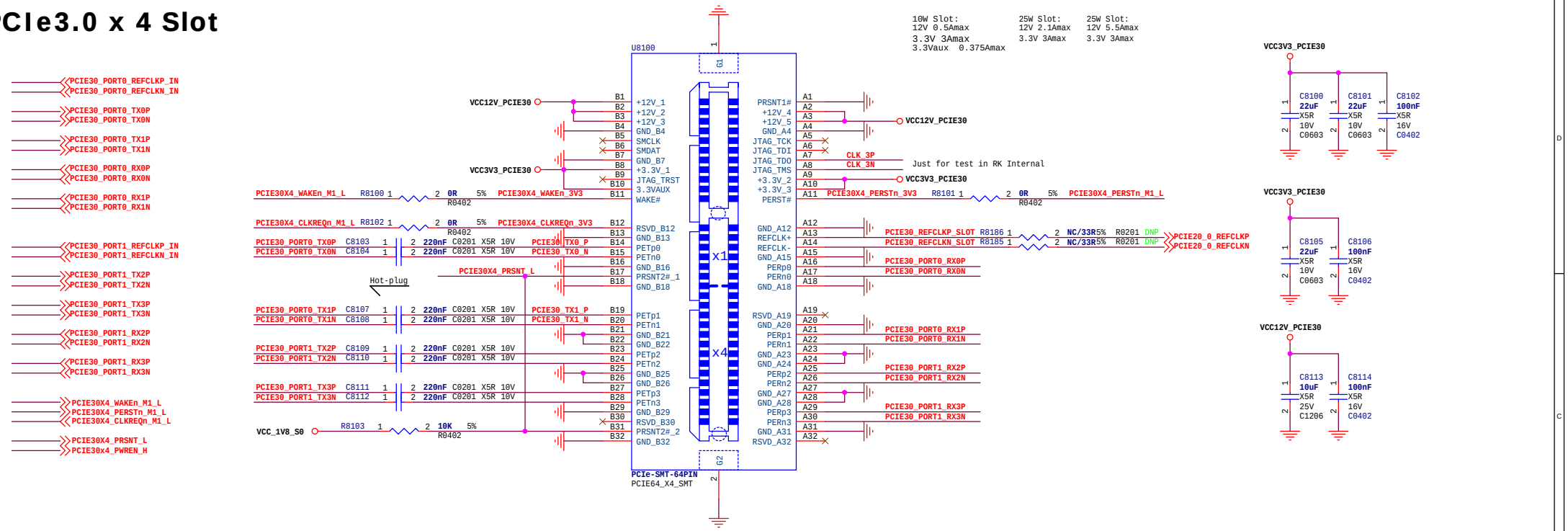


SPEAKER

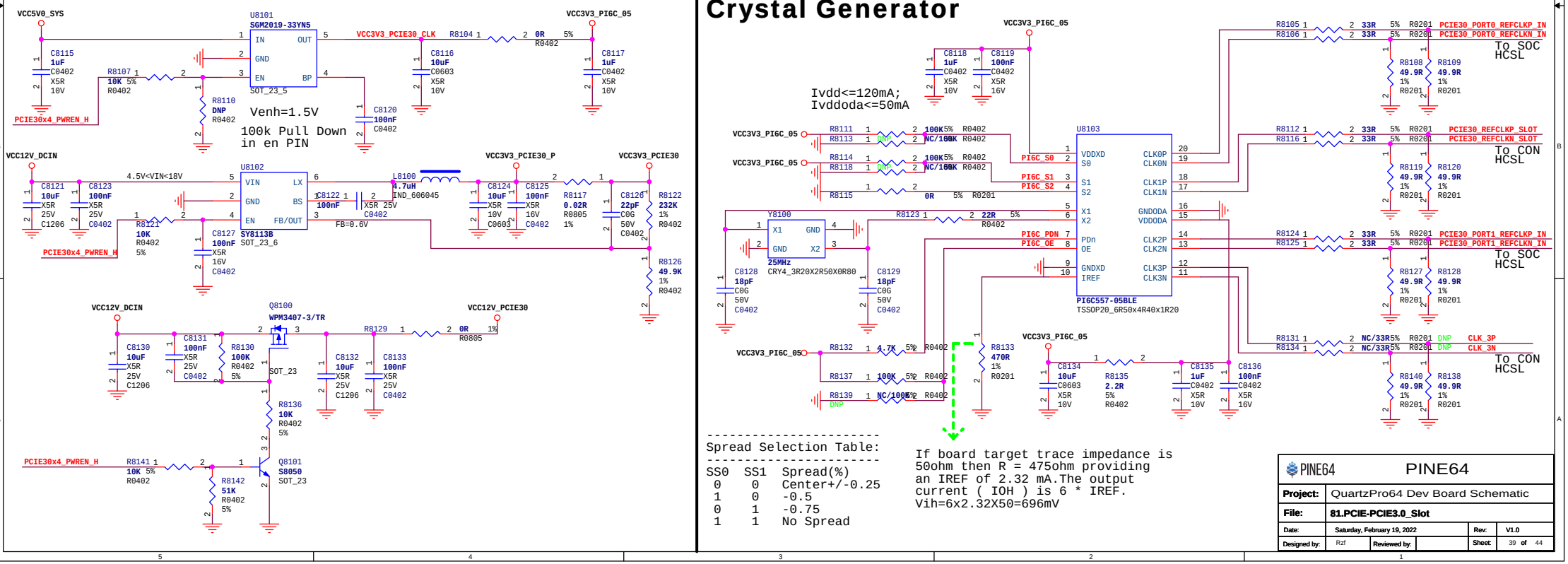


PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	Audio Codec-ALC5651				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	38 of 44

PCIe3.0 x 4 Slot



Crystal Generator



Spread Selection Table:

SS0	SS1	Spread(%)
0	0	Center+/-0.25
1	0	-0.5
0	1	-0.75
1	1	No Spread

If board target trace impedance is 50ohm then R = 475ohm providing an IREF of 2.32 mA.The output current (IOH) is 6 * IREF.
Vih=6x2.32X50=696mV

Project:	QuartzPro64 Dev Board Schematic
File:	81.PCIE-PCIE3.0_Slot
Date:	Saturday, February 19, 2022
Rev:	V1.0
Designed by:	Rzf
Reviewed by:	
Sheet:	39 of 44

SATA3.0

SATA30_0_TXP
SATA30_0_TXN
SATA30_0_RXP
SATA30_0_RXN

SATA30_0_TXP → J8300 pin 2 (TXP)
SATA30_0_TXN → J8300 pin 3 (TXN)
SATA30_0_RXN → C8302 1 — 2 10nF X5R 10V C0201 → SATA1RXN → J8300 pin 5 (RXN)
SATA30_0_RXP → C8303 1 — 2 10nF X5R 10V C0201 → SATA1RXP → J8300 pin 6 (RXP)

J8300: 1 GND1, 2 TXP, 3 TXN, 4 GND2, 5 RXN, 6 RXP, 7 GND3, 8 GND4, GND5, 9 SATA30_7P_V_DIP
SATA30_7P_V_DIP

PCIE20_1_TXP
PCIE20_1_TXN
PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN

PCIE20_1_TXP → C8310 1 — 2 NC/10nF X5R 10V C0201 DNP → SATA30_1_TXP → J8302 pin 2 (TXP)
PCIE20_1_TXN → C8311 1 — 2 NC/10nF X5R 10V C0201 DNP → SATA30_1_TXN → J8302 pin 3 (TXN)
PCIE20_1_RXN/SATA30_1_RXN → C8312 1 — 2 NC/10nF X5R 10V C0201 DNP → SATA30_1_RXN → J8302 pin 5 (RXN)
PCIE20_1_RXP/SATA30_1_RXP → C8313 1 — 2 NC/10nF X5R 10V C0201 DNP → SATA30_1_RXP → J8302 pin 6 (RXP)

J8302: 1 GND1, 2 TXP, 3 TXN, 4 GND2, 5 RXN, 6 RXP, 7 GND3, 8 GND4, GND5, 9 SATA30_7P_V_DIP
SATA30_7P_V_DIP

Note:
The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA_POWER

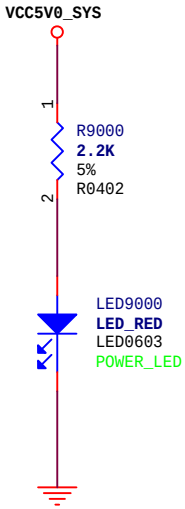
VCC5V0_SYS → R8300 0R R1206 5% → C8304 120uF SVPF 20V E_C6 + C8305 100nF X5R 16V C0402 → J8301 pin 1 (+5V)
J8301 pin 2 (GND1), pin 3 (GND2)
VCC12V_DCIN → R8301 0R R1206 5% → C8306 100uF SVPF 25V E_E7 + C8307 100nF X5R 25V C0402 → J8301 pin 4 (+12V)

J8301: NC/SATA_IDE_DIP_4Pin
SATA-IDE4M_5R08_DIP

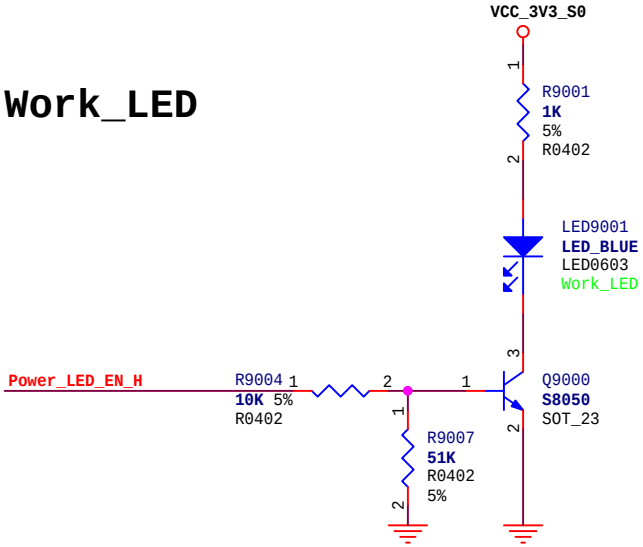
PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**83.SATA-SATA3.0 Slot_7P**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Default	Sheet:	40 of 44

Power_LED_EN_H

Power_LED

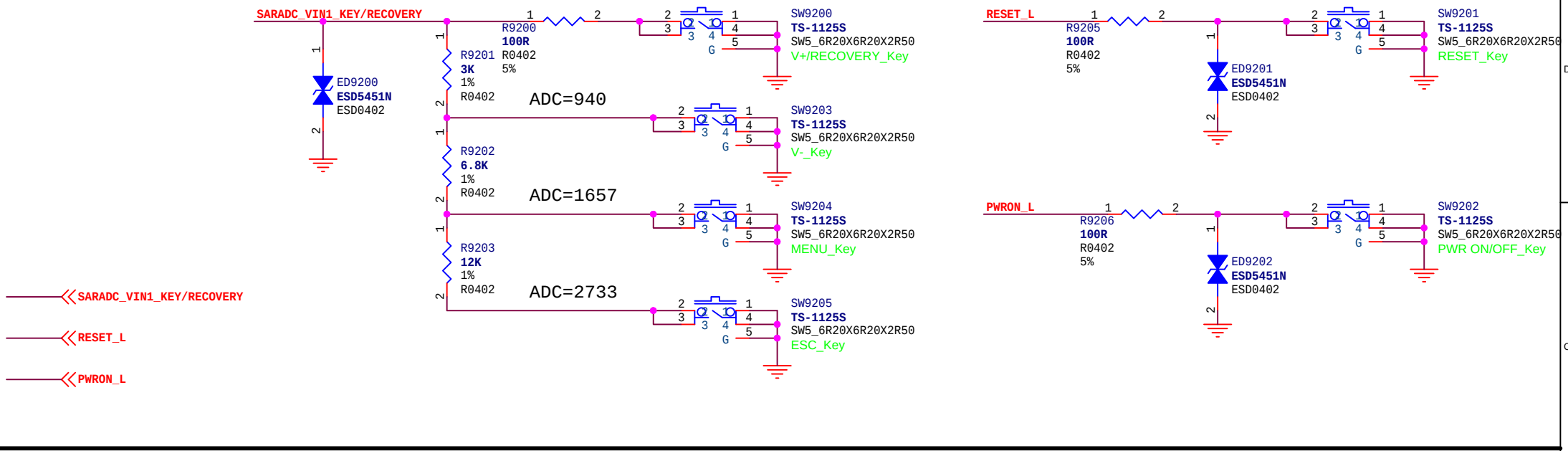


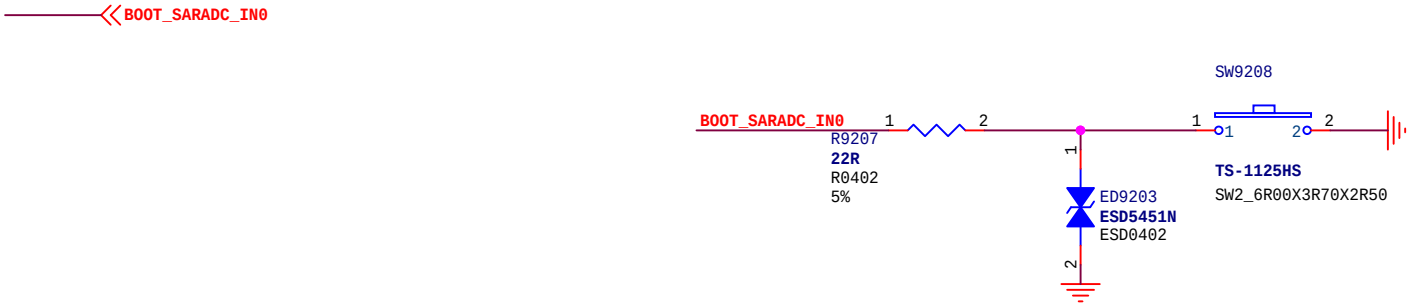
Work_LED



PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**90.LED**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	41 of 44

KEY

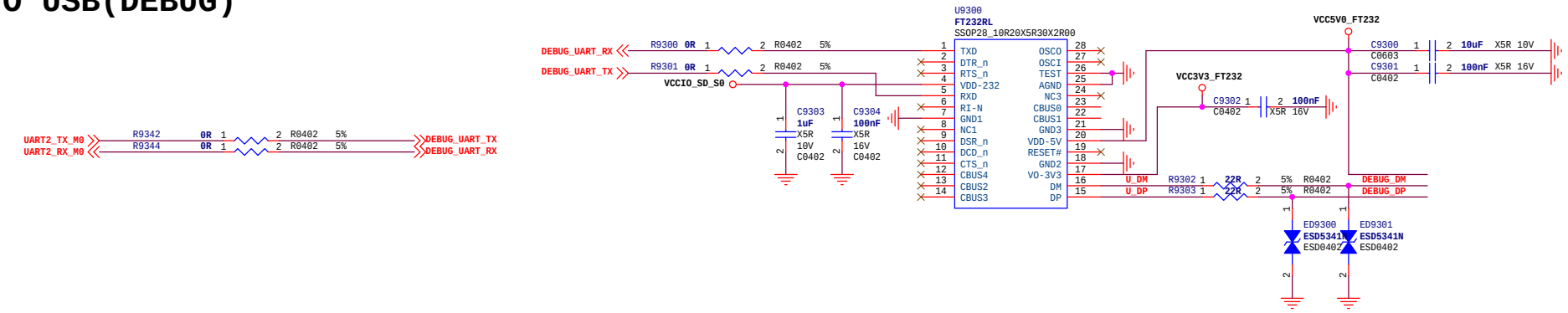




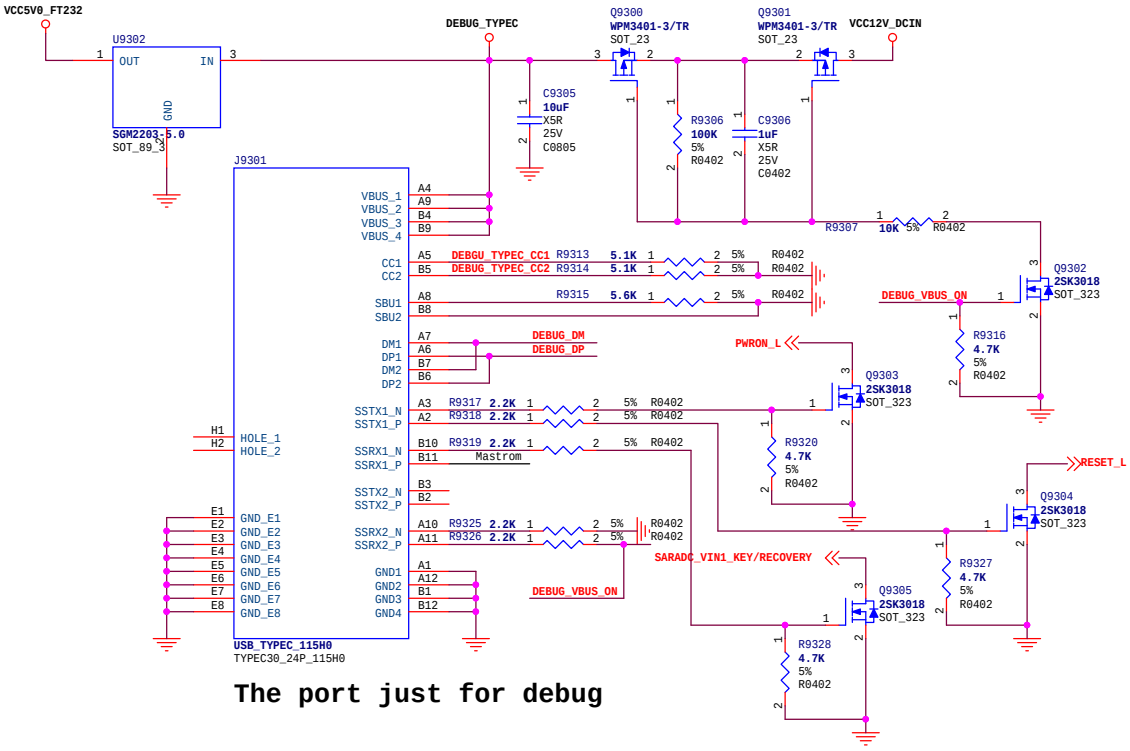
Note:
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**92.KEY Array**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	42 of 44

UART TO USB(DEBUG)



Extboard Debug Port



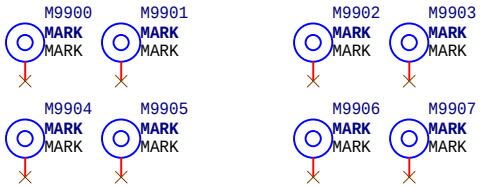
The port just for debug

PINE64	PINE64		
Project:	QuartzPro64 Dev Board Schematic		
File:	93.Debug UART/JTAG Port		
Date:	Tuesday, February 15, 2022	Rev:	V1.0
Designed by:	Rzf	Reviewed by:	Sheet: 43 of 44

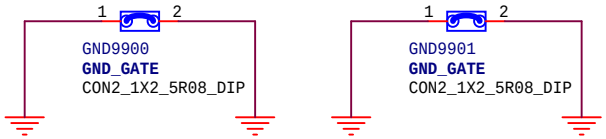
Mark

TOP Mark

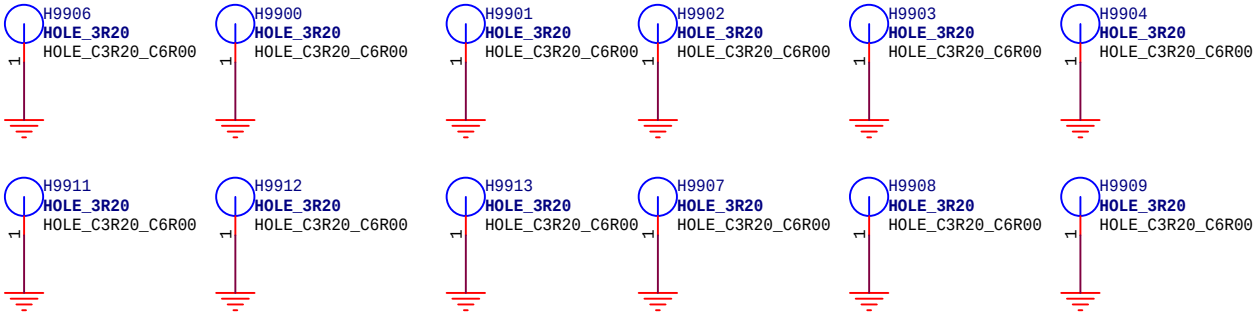
BOTTOM Mark



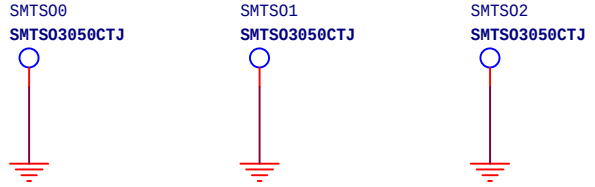
GND GATE



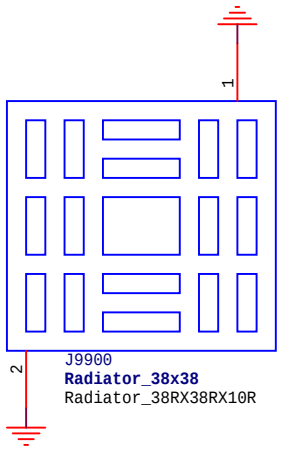
HOLE



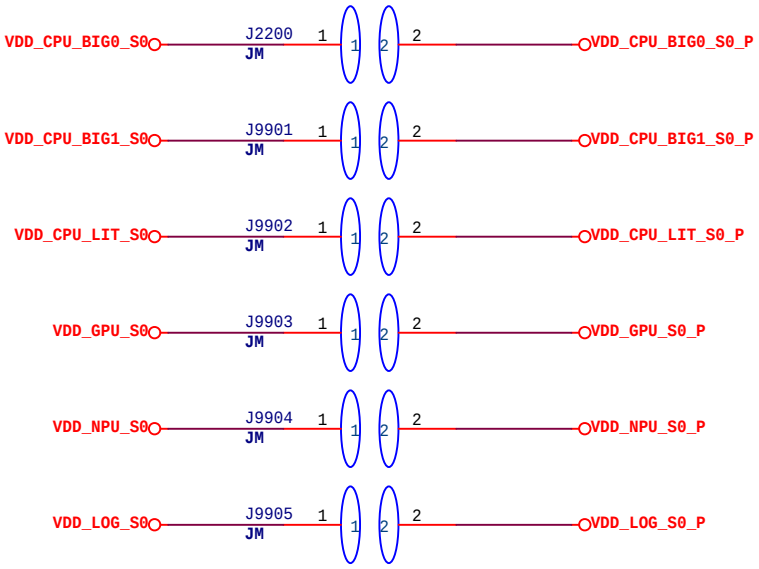
CAMERA HOLE

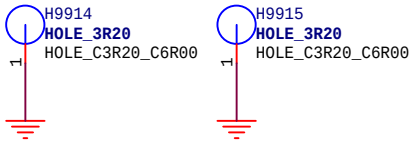


HEATSINK



FAN:8CMX8CM





PINE64	PINE64				
Project:	QuartzPro64 Dev Board Schematic				
File:	**99.Mark/Hole/Heatsink**				
Date:	Tuesday, February 15, 2022			Rev:	V1.0
Designed by:	Rzf	Reviewed by:		Sheet:	44 of 44